A homebrew two-minute alarm circuit for a roll-up door openings

A roll-up door and an adjacent man door in a warehouse are used frequently. Often, the operators are careless and leave one or the other door open longer than necessary, allowing heated or cooled air inside to escape. Some means is needed to remind the operators to shut the doors. Neither door should be left open for longer than two minutes.

The device described below sounds a siren if either door is left open for longer than two minutes. To be precise, the two minute grace period starts when either door is opened. The grace period continues, but does not re-start, if the other door is also opened. Unless both doors are closed by the end of the grace period, the siren starts to sound. The siren continues to sound until both doors are closed.

For convenience, the siren is mounted on the enclosure of the device. The siren is a standard 12VDC 20W siren, which was purchased at a local Princess Auto store. It is loud.

The device receives its inputs from two common "door open/close" sensors, one mounted on each door.

> Aside
>
> There are two basic types of "door open/close" sensors: (i) single-pole single-throw (SPST) reed switches and (b) magnetic switches whose resistance varies with the proximity of a magnet. Each type comes in two configurations: (i) normally-closed and (ii) normally-open.
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> SPST switches contain a steel reed whose position either shorts out two internal contacts or leaves them unconnected. They are easy to use, but not as sensitive as magnetic switches. The circuit described below assumes magnetic switches are used, but will work equally well with simple SPST magnetic reed switches.
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> The normally-open (NO) configuration refers to a sensor whose resistance is high (or infinite) when the sensor and its magnet are in close proximity. The resistance goes low (zero, in the case of an SPST sensor) when the magnet is withdrawn, as it will be when the door is opened. The normally-closed (NC) configuration has low (or zero) resistance when the two pieces are in close proximity. The resistance goes high (infinite, in the case of an SPST sensor) when the magnet is withdrawn.
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> The circuit described below can be connected to either NO or NC sensors.

One of the sensors is mounted on the top edge of the door frame of the man door and its corresponding magnet is mounted on the top edge of the door itself. The two pieces are mounted so that they are positioned face-to-face when the door is closed. The second, similar, sensor is mounted on the roll-up door. In this case, the magnet is fixed to the top edge of the roll-up door and its corresponding sensor is mounted on the adjacent wall where it will be in close proximity to the magnet when the roll-up door is closed.

A logic circuit merges the inputs from the two sensors through a NAND gate, whose output triggers a timing circuit. The timing circuit controls the gate of a power MOSFET. The siren is wired in series with the MOSFET's source-drain loop and sounds when the MOSFET conducts.

It should be noted that any break in the wiring connecting the sensors to the logic circuit has the same effect as an open door, namely, that the siren will sound. This will ensure that an inoperative circuit is detected quickly.

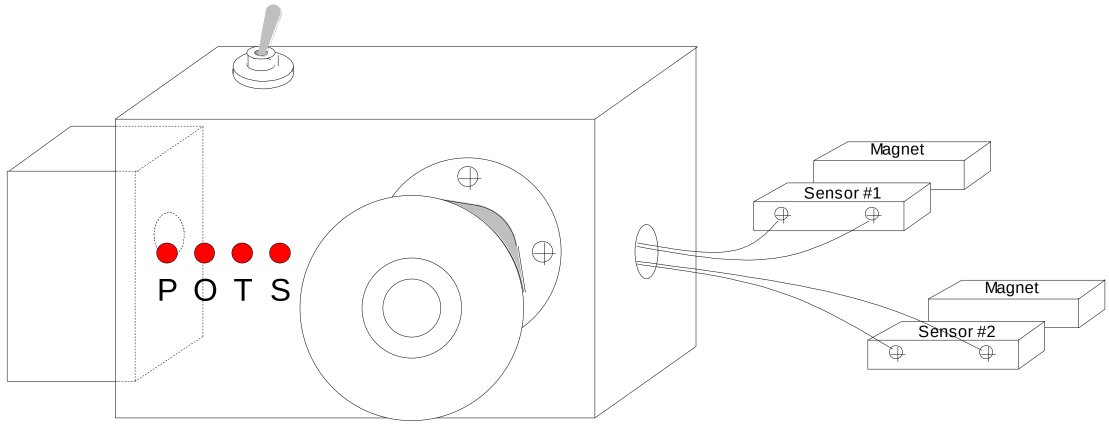
The device is powered by 120VAC, which is delivered to the device through a metal electrician's utility box mounted on the side of the enclosure. A small transformer and full-wave rectifier provide 12VDC.

Circuit diagrams

Appendix "A" attached hereto is the schematic diagram of the circuit (the "Schematic"). There are two single-sided printed circuit boards. "PCB#1" is the logic circuit. The copper trace layer and silkscreen layer for PCB#1 are shown in the see-through view in Appendix "B". PCB#2 is a small circuit board which holds the four LED indicator lights. It is bolted directly to the front panel of the enclosure. The copper trace layer and silkscreen layer for PCB #2 are shown in the see-through view in Appendix "B". The Schematic and PCBs were prepared using ExpressPCB, a program which can be downloaded for free on the internet.

The enclosure

The transformer and circuit boards are mounted inside a 9.4"×6.3"×3.5" plastic enclosure (Digikey part # HM930-ND). The finished enclosure looks something like this.

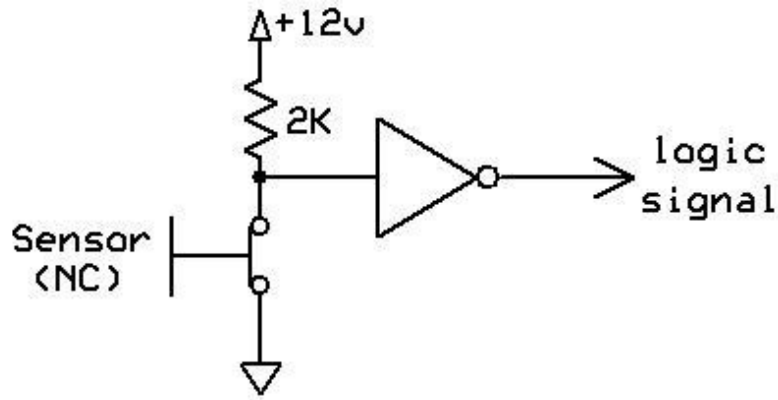


The metal electrician's utility box, in which wires from the building's AC mains are connected to the leads of the transformer's primary winding, is mounted on the left side of the enclosure. The toggle switch (optional) which turns the device on and off is mounted on the top.

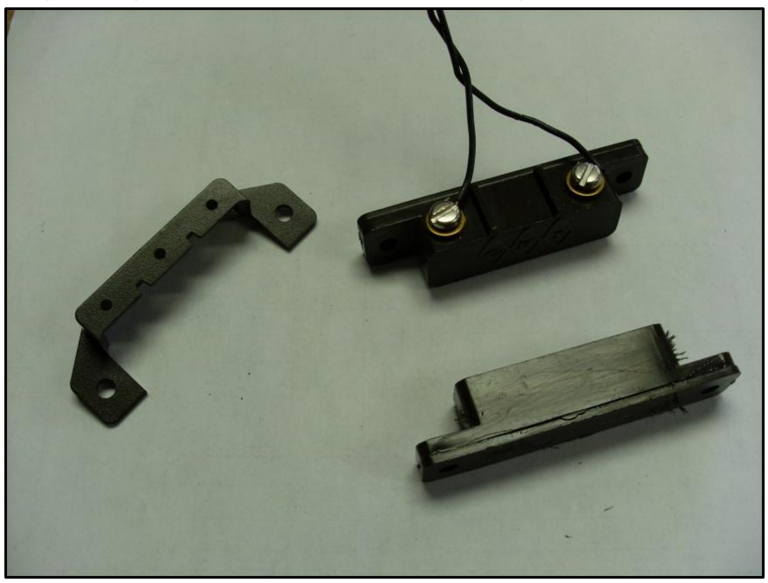
The four LED indicator lights and the siren are mounted on the front panel. The two pairs of wires which connect to the two sensors exit from the enclosure on its right side. The enclosure itself is mounted on the building's wall a convenient distance away from the tracks of the roll-up door.

The sensors

The sensors used in this devise were manufactured by George Risk Industries (GRI) and are GRI's series 29. Experiment showed that the resistance between the two contacts of the sensor was 1.4KΩ when the magnet was nearby and 2.8KΩ when the magnet was removed. These resistances were "digitized" to serve as inputs to a 12V logic circuit as follows:



When the door is closed and the magnet is near the sensor, the sensor's 1.4KΩ resistance divides the 12V supply voltage in the ratio 2:1.4, giving 4.9V at the input to the inverter. When the door is open and the magnet is far away, the sensor's 2.8KΩ resistance divides the 12V supply voltage in the ratio 2:2.8, giving 7.0V at the input to the inverter. The inverter changes state at an input voltage of 6.0V. In the first case (door closed and magnet near-by), the inverter's output will 12V. In the second case (door open and magnet far away), the inverter's output will be zero volts. The following photograph shows the three parts of a typical sensor.



The magnet is contained inside the piece at the bottom of the photograph. You may be able to see a few magnetic filings drawn to the right end of this piece. The sensor, with two wires connected, is at the top of the photgraph. The odd-shaped piece at the left of the photograph is merely a cover for the sensor. It is placed over the sensor when the sensor is mounted to the door frame or wall. It covers the screws for the hook-up wires, thwarting unauthorized disconnection.

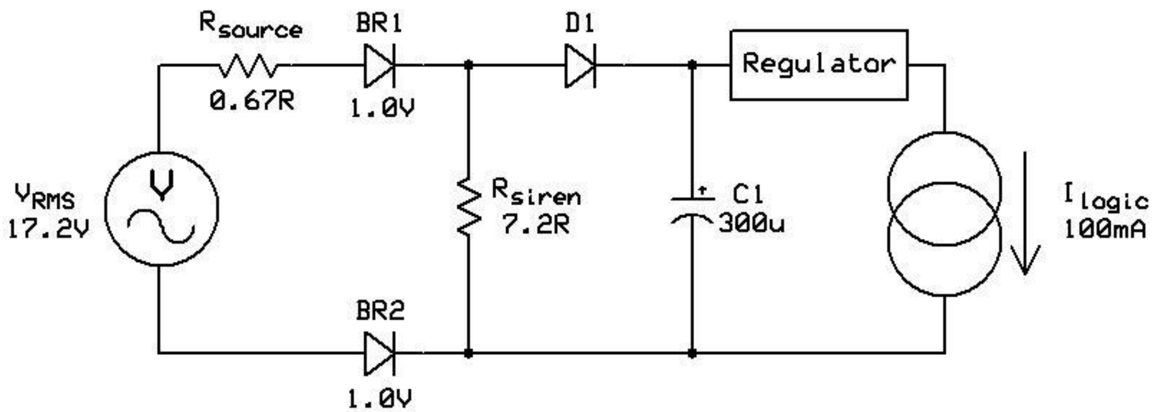
The power supply

A BX armoured cable runs from an electrical panel in the building to a metal utility box mounted on the left side of the enclosure. The armoured cable enters the utility box using a standard BX connector. The utility box is connected to the enclosure, and secured to it, using a standard ROMEX connector. Unlike a BX connector, a ROMEX connector is suitable for passing plastic-covered wires like those found on a small power transformer. One lead of the primary winding of transformer T1 (which is mounted inside the enclosure) passes through the ROMEX connector and into the utility box. The other lead of the transformer is soldered to one contact of the SPST on-off toggle switch (S1) mounted on the top of the enclosure. A hook-up wire from the other contact of the SPST toggle switch also passes through the ROMEX connector and into the utility box. The utility box is physically attached to the enclosure simply to provide a convenient place for the AC mains to be connected to the primary leads of the transformer.

The secondary winding of the transformer (Digikey part # HM533-ND) is rated for power of 35.2VA at 16 VAC. The secondary winding has a center tap, which is ignored in this circuit.

The secondary winding of T1 is wired to the two AC terminals of bridge rectifier BR1. The rectified AC from the bridge rectifier is delivered to two separate sub-circuits. It is delivered to a three-terminal voltage regulator, which provides regulated 12VDC for the logic circuit. The rectified AC is also delivered, separately and without any regulation, to power transistor Q1, which powers the siren when it sounds. The siren works well using rectified AC – it does not need filtered DC. Powering the siren with rectified AC means that the voltage regulator circuit can be made smaller – it only needs to power the logic circuit. For this purpose, a relatively small filter capacitor (C1) is sufficient. A 300µF capacitor was used. I will take a few paragraphs to confirm that this is an appropriate value, being neither too high nor too low.

Let's take a look at the power supply when it is most heavily loaded, which will be when the siren is sounding. The essential features of the power supply when the siren is sounding are shown in the following figure.



The secondary winding of the transformer has been modeled as an ideal alternating voltage source, having a root-mean-square (RMS) voltage of V_{RMS}, in series with an internal "source" resistance R_{source}. The values of these two parameters were determined by the following experiment. An AC voltmeter was used to measure the no-load voltage over the secondary winding of transformer. The voltage measured was $V_{RMS} = 17.2\text{V}$. (Note that the peak voltage of a sinusoidal waveform is equal to its RMS voltage multiplied by the factor $\sqrt{2}$. Therefore, the no-load voltage waveform over the secondary winding is a sinusoid having a peak voltage equal to $V_{peak} = \sqrt{2}V_{RMS} = 24.3\text{V}$.) Then, a 7.0Ω resistor was attached across the secondary winding. The voltage measured over this resistor was $V_{RMS\ loaded} = 15.7\text{V}$. The current flowing through the resistor in this configuration can be computed as $I_{RMS\ loaded} = 15.7\text{V}/7.0\Omega = 2.24\text{A}$. Since the voltage drop over the transformer's internal resistance is equal to $\Delta V_{RMS} = 17.2\text{V} - 15.7\text{V} = 1.5\text{V}$, we can use Ohm's law, which applies to RMS values as well as DC values, to calculate the internal, or "source", resistance as $R_S = \Delta V_{RMS}/I_{RMS\ loaded} = 1.5\text{V}/2.24\text{A} = 0.67\Omega$.

The two diodes BR1 and BR2 are two of the four diodes inside the bridge rectifier. Assume that the circuit is shown during one of the positive pulses of the input sinusoidal waveform, so that these two diodes are conducting. During a negative pulse, it will be the other pair of diodes inside the bridge rectifier which conduct, but the circuit will still look the same, with two conducting diodes. Of course, there will be a short interval of time between successive pulses in the input waveform when the voltage over the secondary winding is so close to zero that neither pair of diodes conducts. The duration of this interval is governed by the forward voltage drop over the diodes. The datasheet for the bridge rectifier (Digikey part # RS403GL-BPMS-ND) gives a maximum forward voltage drop of 1.0V per leg at a forward current of 3A and an ambient temperature of 25°C. At lower forward currents or at higher temperatures, the forward voltage drop will be even less. We will model the diodes, <u>when they conduct</u>, as constant 1.0V voltage drops.

The siren is modeled as a resistor. This is tantamount to assuming that the siren is 100% efficient, so that all of the electrical power applied to it is dissipated as sound or heat. One consequence of this assumption is that the siren's coil does not return any energy to the circuit, which is to say that its inductance is negligible. For analysis purposes, note that the siren has a power rating of 20W at a DC voltage of 12V. The current flowing through the siren under these conditions will be equal to $I = Power/V = 20\text{W}/12\text{V} = 1.67\text{A}$. The siren's equivalent resistance can then be calculated using Ohm's law as $R_{siren} = 12\text{V}/1.67\text{A} = 7.2\Omega$.

Now, let's turn to the filter capacitor C1. Diode D1 prevents this capacitor from discharging through the siren. The voltage over the siren tracks the voltage from the bridge rectifier, which is a rectified sinusoid, ranging from zero up to the peak voltage of approximately 24.3V. There are times when the voltage over the secondary winding is less than the voltage over the filter capacitor, during which diode D1 will prevent the "backflow" of charge. C1 can and will discharge through the regulator and the load, but never through the siren.

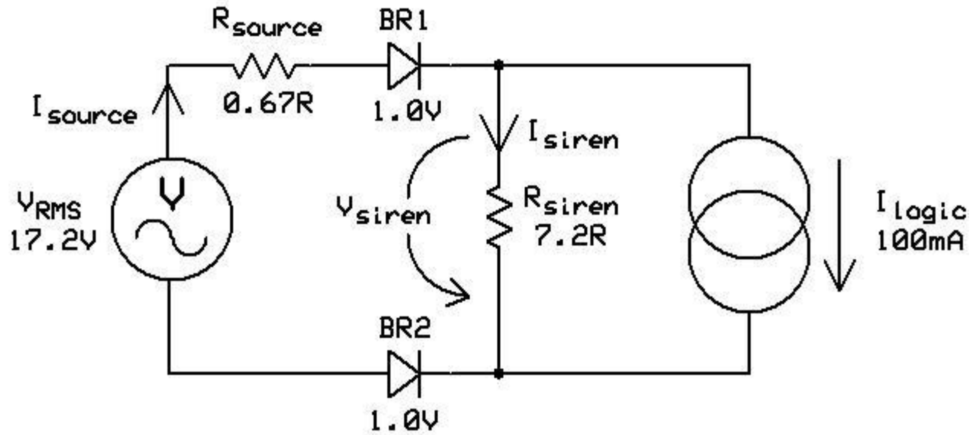
At this point, we do not know anything about the logic circuit. Let us assume, for this preliminary analysis, that the logic circuit will consume 100mA or less of current. This is an educated guess, based on the expectation that the primary users of energy in the logic circuit are two magnetic sensors, three or four logic gates, a timer chip and four LEDs.

1. The two sensors have been biased to consume a total of about 10mA. We saw above that each sensor circuit consists of a series resistance of between 3.4KΩ and 5.8KΩ over the supply voltage of 12V, so each circuit will draw between 2mA and 3.5mA of current. Twice this rounds up to about 10mA.
2. If the logic gates are CMOS chips, they will consume about 3mA each. Say another 10mA is used by the gates.
3. An LM555 timer chip will consume another 10mA.
4. We can bias the LEDs with 1KΩ resistors so they consume 10mA or so apiece when lit.

All together, this adds up to 80mA. The voltage regulator will also dissipate power, but only in connection with the voltage drop from its input terminal to its output terminal. The additional current consumed by the regulator itself is negligible. But, we will need to ensure that the voltage drop from the input terminal to the output terminal does not fall below the "drop out" voltage of the regulator. I will say more about this issue below.

In the circuit drawn above, the logic circuit is shown as a constant current sink of 100mA. (Many readers will recognize that I have actually used the symbol for a current source for the logic circuit, but I intend it to be understood that it is a current sink.)

Now, we know that the current flowing through the siren (approximately 2A at 12V) is much greater than the flowing into the logic circuit (approximately 100mA), perhaps 10 or 20 times greater. As a first approximation for an analysis, we can ignore the components which support the supply of current to the logic circuit. More specifically, we can ignore the filter capacitor C1, the blocking diode D1 and the regulator. This simplified circuit is shown below.



Let me explain the effect of ignoring the supporting components. Although the filter capacitor has been ignored in the simplified circuit, the logic circuit and the power it consumes has not. The logic circuit continues to be modeled as a constant current sink, absorbing 100mA continuously. The job of the filter capacitor is to provide current to the logic circuit when the voltage of the instantaneous input voltage is too low to do so, and then to replenish its energy when the instantaneous input voltage is at higher values. In a sense, the filter capacitor does not affect the average load on the transformer; it merely affects the timing by taking in extra energy during the peaks and sending it to the logic circuit during the valleys. The simplified circuit shown above ignores these timing fluctuations and models the logic circuit as a constant demand.

In the figure, the instantaneous currents flowing through the siren and from the secondary winding are labeled I_{siren} and I_{source}, respectively. There is only one node and the sum of all currents flowing through it must be zero. Therefore, we can write down the first circuit equation as:

$$I_{source} = I_{siren} + I_{logic} \quad (1)$$

I have also identified in the figure the instantaneous voltage over the siren as V_{siren}. Although I did not identify it specifically in the figure, let us refer to the instantaneous voltage over the secondary winding as V_{source}. Of course, the RMS value of V_{source} is $V_{RMS} = 17.2\text{V}$, which has already been described. The instantaneous voltage drops over the source resistor and the two bridge rectifier diodes are related to the other voltages by:

$$V_{source} - (I_{source} \times R_{source}) - 2\text{V} = V_{siren} \quad (2)$$

Note that Ohm's law has been applied to the source resistor to calculate the voltage over it. The voltage drops over the two diodes are constant, at one volt apiece.

Since we have modeled the siren as a resistor, we can also apply Ohm's law to it. We get:

$$V_{siren} = I_{siren} \times R_{siren} \quad (3)$$

Finally, we have characterized the logic circuit as a constant current sink, so we can write:

$$I_{logic} = 0.1\text{A} \quad (4)$$

We can combine these four equations by: (i) substituting Equation (4) into Equation (1), (ii) re-arranging Equation (3) to be $I_{siren} = V_{siren}/R_{siren}$, (iii) substituting I_{siren} into Equation (1) and, finally, (iv) substituting Equation (1) into Equation (2). We get:

$$V_{source} - \left[\left(\frac{V_{siren}}{R_{siren}} + 0.1\text{A}\right) \times R_{source}\right] - 2\text{V} = V_{siren} \quad (5)$$

After a bit of algebra, Equation (5) can be re-arranged as:

$$V_{siren} = \frac{V_{source} - 2\text{V} - (0.1\text{A} \times R_{source})}{1 + \frac{R_{source}}{R_{siren}}} \quad (6)$$

If we isolate the dependence on V_{source}, we get:

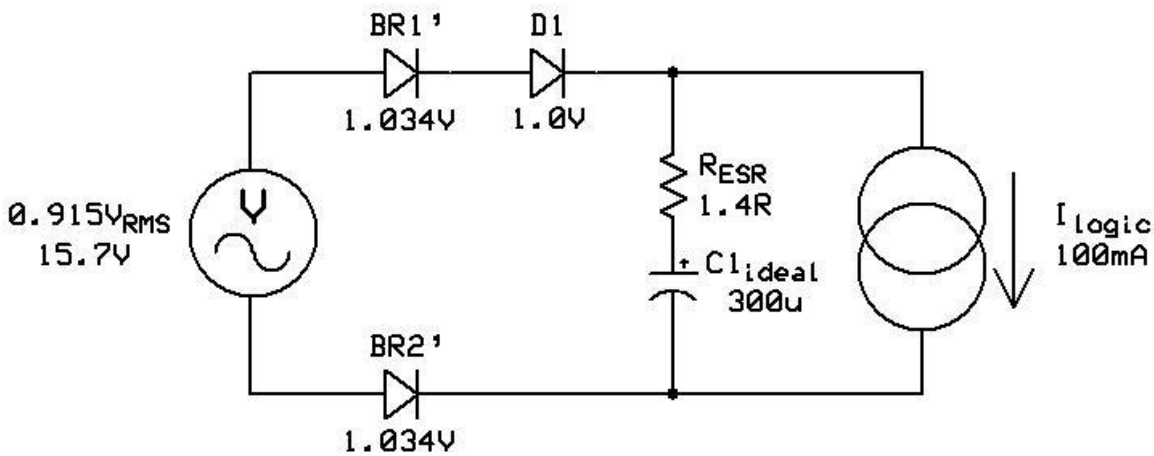
$$V_{siren} = \left[\frac{1}{1 + \frac{R_{source}}{R_{siren}}}\right] V_{source} - \left[\frac{2\text{V} + (0.1\text{A} \times R_{source})}{1 + \frac{R_{source}}{R_{siren}}}\right] \quad (7)$$

When we substitute the values of the resistances, we get:

$$V_{siren} = 0.915V_{source} - 2.067\text{V} \quad (8)$$

If $V_{source} > 2.067\text{V}/0.915$, which is equal to 2.26V, the left-hand-side of Equation (8) is algebraically positive. On the other hand, if $V_{source} < 2.26\text{V}$, the left-hand side of Equation (8) is negative. Physically, that cannot be. V_{siren} cannot be negative. This conundrum is resolved by revisiting one of the initial assumptions we made before analyzing the circuit: that the two diodes are conducting. If the diodes are not conducting, then circuit Equation (2) and the following equations which depend on it do not apply. The transition point occurs at $V_{source} = 2.26\text{V}$. When $V_{source} \leq 2.26\text{V}$, no current flows through the siren.

We can interpret Equation (8) as follows: the instantaneous voltage over the siren is directly proportional to the instantaneous voltage over the secondary winding, less a constant voltage drop. From an electrical point-of-view, therefore, we could replace the siren in the circuit above with an equivalent voltage source consisting of: (i) an ideal alternating voltage source having a magnitude of 91.5% of the secondary winding voltage, (ii) accompanied by two new diodes (labeled BR1' and BR2'), each having a voltage drop equal to one-half of 2.067V. The following figure shows the power supply from the point-of-view of the logic circuit.

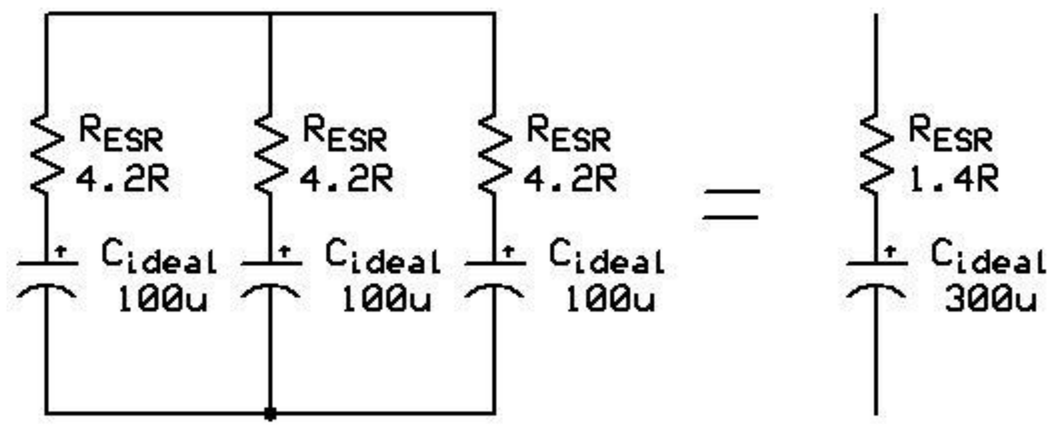


Note that I have brought filter capacitor C1 and blocking diode D1 back into the circuit. Since the RMS voltage of the secondary winding's waveform was 17.2V, the RMS voltage over the siren is 91.5% as much, or 15.7V.

Now, let's turn our attention once more to the filter capacitor. Capacitor C1 is constructed from three 100µF capacitors wired in parallel. (I have a great many of these capacitors in my spare parts box.) Wiring capacitors in parallel has the effect of adding their capacitances. However, real capacitors are accompanied by a certain amount of internal resistance, which is customarily represented in a circuit diagram as a resistance placed in series with the ideal capacitance. This resistance is called the equivalent series resistance (ESR) of the capacitor. The individual capacitors (C1A, C1B and C1C) which make up C1 are miniature electrolytic capacitors rated to withstand 25V (Digikey part # 565-1059-ND). The datasheet for these capacitors gives their individual equivalent series resistance (ESR) parameter as $\tan\delta = 0.16$. At the driving frequency of 60Hz, the capacitive reactance of these capacitors is equal to $X_C = 1/2\pi fC = 1/(2\pi \times 60 \times 100\mu) = 26.5\Omega$. The ESR resistance of each of these capacitors is therefore equal to $R_{ESR} = \tan\delta \times X_C = 0.16 \times 26.5\Omega = 4.24\Omega$.

The ESR parameter is quoted as a trigonometric tangent for a purpose. The voltage and current of a capacitor are 90° out-of-phase. The voltage and current of the equivalent series resistance are in phase. In a graphical analysis of a circuit, an out-of-phase voltage and current would be represented by vectors pointing at right angles to each other. When such a "reactive" pair of vectors is combined with the parallel vectors of a "resistive" pair of in-phase vectors, the resultant vectors lie at various angles, which are most easily calculated using trigonometry.

We need to figure out how the capacitors are combined when they are wired in parallel. We know that the capacitances should be added together, but what about their equivalent series resistances? The equivalent configuration is shown in the following figure.



On the left, each branch represents one of the physical capacitors. Each branch is identical. The reactance of the leftmost branch ($branch1$) can be represented as a complex number in the following way:

$$X_{branch1} = R_{ESR} + \frac{1}{j\omega C_{ideal}} \quad (9)$$

where j is the imaginary number and ω is the angular frequency, equal to $2\pi f$, where f is the temporal frequency in Hertz. For a resistor, reactance and resistance are identical, since the voltage and current are in phase. For a capacitor or inductor, reactance and resistance are similar concepts, but not identical. It is most useful to think of reactance as the resistance to alternating current. Like resistance, reactance is measured in Ohms. But, since voltages and currents are not in phase in capacitors and inductors, some means is needed to measure the extent to which the voltages and currents are out of phase. One way to do this is to use angles, as we did above for the ESR parameter of the capacitors. Another way is to use complex numbers. The imaginary number can be thought of as a vector pointing at right angles to the real number "1". Because of this, complex numbers preserve exactly the same trigonometric information as simple angles.

The reactances of two branches of a circuit wired in parallel can be combined in exactly the same way as simple resistances, namely, R1‖R2=R1R2/(R1+R2). For example, the reactance of the two leftmost branches in the circuit above is equal to:

$$X_{branch1||branch2} = \frac{\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)}{\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right) + \left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)}$$

$$\rightarrow X_{branch1||branch2} = \frac{1}{2}\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right) \quad (10)$$

The algebra is greatly simplified because the branches are identical. Now, let's add the third branch to the parallel combination of the two leftmost branches:

$$X_{branch1||branch2||branch3} = \frac{\frac{1}{2}\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)}{\frac{1}{2}\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right) + \left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)}$$

$$\rightarrow X_{branch1||branch2||branch3} = \frac{1}{3}\left(R_{ESR} + \frac{1}{j\omega C_{ideal}}\right)$$

$$\rightarrow X_{branch1||branch2||branch3} = \frac{R_{ESR}}{3} + \frac{1}{j\omega(3C_{ideal})} \quad (11)$$

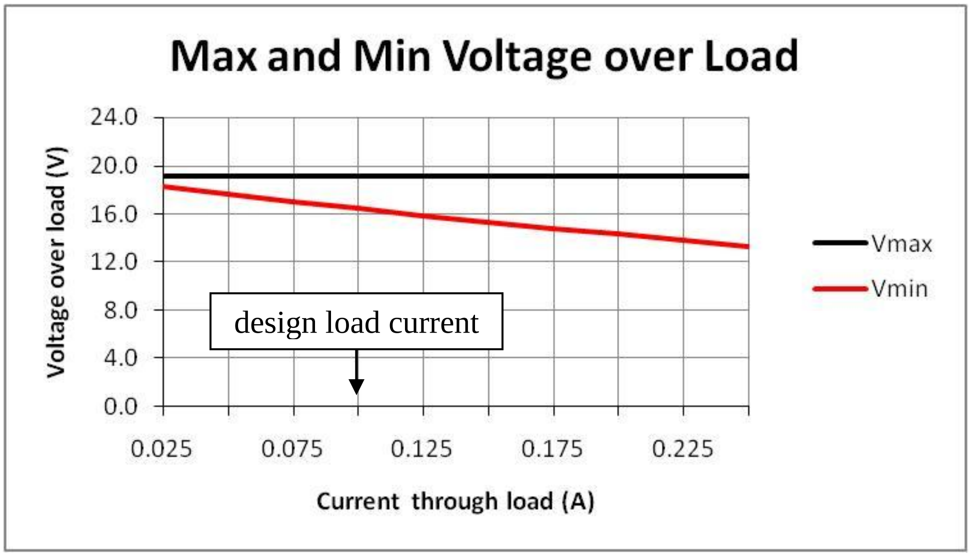
So, the equivalent circuit of three physical capacitors in parallel is an ideal capacitance having three times the individual capacitance together with a series resistance having one-third of the individual ESR. This equivalent circuit is shown on the right hand side of the figure above.

I have also added to the revised power supply circuit shown above an additional piece of information about blocking diode D1. The datasheet for this diode (Digikey part # 1N5402DICT-ND) shows that it has a maximum forward voltage drop of 1.0V at a forward current of 3A and an ambient temperature of 25°C. At lower forward currents or at higher temperatures, the forward voltage drop will be even less. To be conservative in the analysis, we will assume that diode D1 is a constant voltage drop of one volt. I have used the adverb "conservative" in the sense of "resulting in the lowest voltage drop over the load".

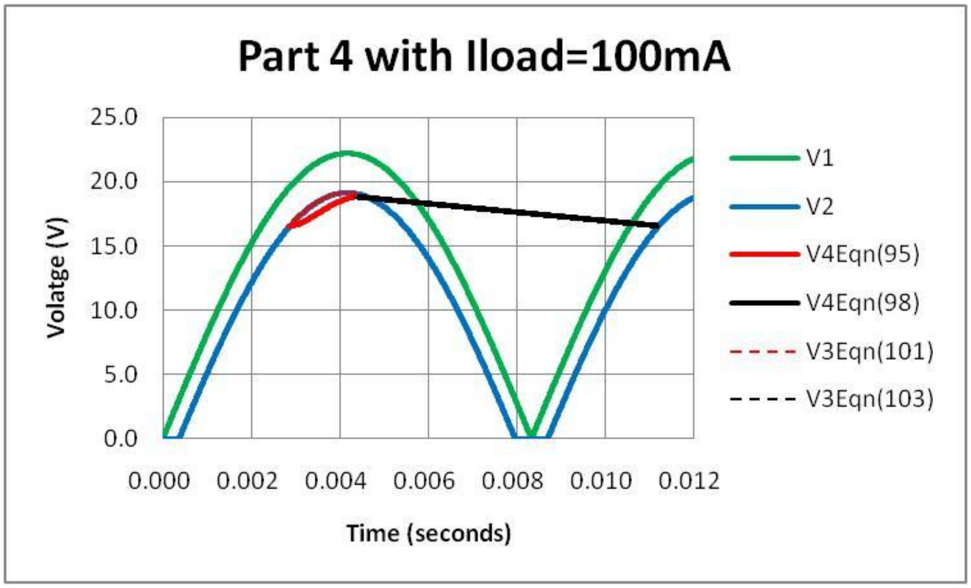
We can analyze the revised power supply circuit shown above using the equations and computer code contained in Part 4 of the accompanying paper *Detailed Analysis of a Full-wave Rectified Power Supply*. The following paragraphs list the parameters needed to execute that analysis using the parameters names described in Part 4 of that paper.

1. $V_{RMS} = 15.7\text{V}$.
2. Internal resistance $R_S = 0$. In the revised circuit, there is no internal source resistance.
3. $C = 300\mu\text{F}$ and $R_{ESR} = 1.4\Omega$.
4. Diode forward voltage drop $V_{BR} = 1.534\text{V}$. The revised power supply circuit contains three diodes which, when in their conducting state, have a total voltage drop of 3.067V. If the three diodes are modeled as a symmetrical pair of diodes, each would have a voltage drop equal to one-half of that, or 1.534V.

The power supply calculations in Part 4 of the accompanying paper were carried out for load currents in a range from 50mA to 250mA. The results are most easily understood in the form of the following chart. The black line represents the maximum voltage applied over the load / logic circuit during a cycle. The red line represents the minimum voltage applied over the load / logic circuit during a cycle.

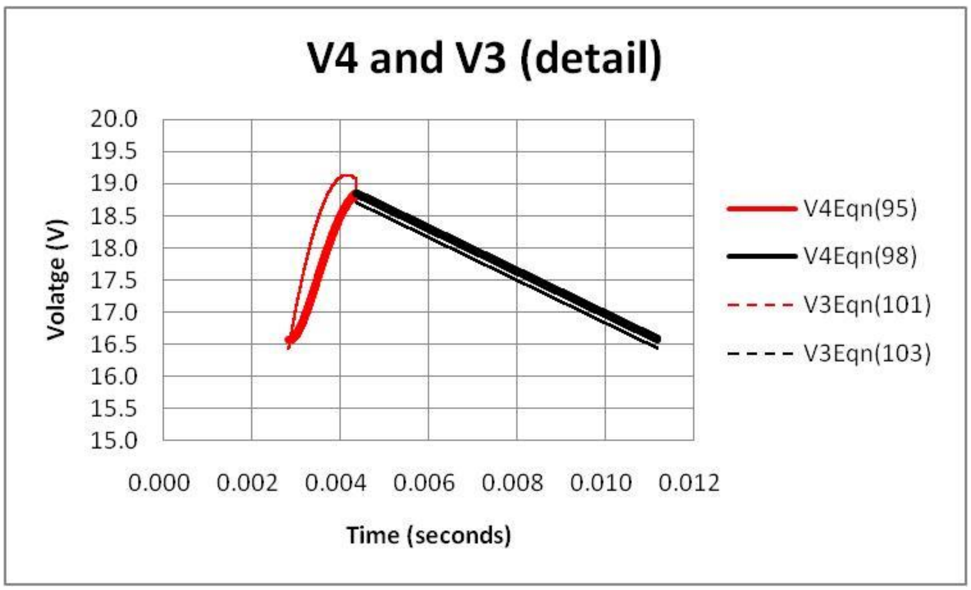


At the design load current (100mA), the minimum and maximum voltages over the load are about 16.2V and 19.2V, respectively. These are the extreme values of the voltages applied over the load during the course of an input voltage pulse. It is useful to look at the actual waveform of the voltage, which is shown in the following figure for the 100mA case.



Time is measured along the horizontal axis starting from an instant when the input voltage is zero. The voltage from the ideal voltage source is shown in green. At a frequency of 60Hz, the duration of one pulse is $1/(2 \times 60) = 8.3\text{ms}$. After 8.3ms, the input voltage has returned to zero and the next pulse begins. The voltage over the output terminals of the bridge rectifier is shown in blue. The bridge rectifier output is a constant voltage drop below the input voltage, but is subject to a minimum of zero. The red and black solid lines (labeled V4 in the chart) are the voltage drop over the ideal capacitance. The red portion of that waveform occurs when the diodes conduct. Generally speaking, the capacitor is recharging during that interval. The black portion of that waveform occurs when the diodes are not conducting and the capacitor discharges through the load. The voltage drop over the load / logic circuit is shown by dotted lines in the graph, in red and black for the diode's conducting and non-conducting intervals, respectively. It can be seen that the voltage drop over the load tracks the voltage drop over the bridge rectifier (in blue) when the diodes conduct and, then, when they do not, follows the capacitor's voltage on the way down.

The dotted lines are not too easy to see in the graph above. They are shown in more detail, with an expanded vertical axis, in the following graph.



As I have said, the voltage drop over the load (dotted red line) follows the bridge rectifier's voltage on the way up, when the diodes conduct. But the voltage drop over the filter capacitor (solid red line) lags behind. The rate at which the filter capacitor recharges is limited by its equivalent series resistance. The time constant at which the capacitor can recharge is given by $\tau = R_{ESR} \times C_{ideal} = 1.4 \times 300\mu = 420\mu\text{s}$. 0.42ms is too long compared with the length of a pulse (8.3ms) for the capacitor to recharge fully in the time given.

The important voltage for our analysis is the minimum voltage over the load at any time during the cycle. The chart shows this minimum to be approximately 16.4V. In the past few paragraphs, I have been using the word "load" as being synonymous with "logic circuit". To be more precise, the leading component in the load is the voltage regulator. We can say, then, that the minimum voltage drop applied over the input terminals of the voltage regulator is 16.4V.

The voltage regulator used has a regulated output voltage of 12VDC at a maximum current of 500mA. The datasheet for the voltage regulator (Digikey part # 497-1464-5-ND) gives a typical dropout voltage of 2V at the maximum output current. To ensure that the regulator does its job, we must ensure that the input voltage is always at least 2V above the output voltage. In other words, we must ensure that the input voltage never falls below 14.0V. A glance at the third-to-last chart above shows that the filter capacitor is able to keep the input voltage above 14V at currents up to about 225mA. Since our design current is 100mA, we should be safe.

This power supply was analyzed using a two-stage process which does introduce some error. Nevertheless, the result seems robust enough for our purpose.

The siren

Let's return for a moment to the siren. Using its 20W rated power and 12V rated voltage, we already calculated above that its equivalent resistance is $R_{siren} = 7.2\Omega$. It is placed in our circuit where it will experience an RMS voltage slightly greater than 12V. Equation (8) above shows that the RMS voltage over the siren will be equal to 91.5% of the RMS voltage of the secondary winding, less 2.1V. This is equal to $V_{RMS\ siren} = 15.7\text{V} - 2.1\text{V} = 13.6\text{V}$. The power the siren will consume at this voltage will be equal to $P_{siren} = (13.6\text{V})^2/7.2\Omega = 25.7\text{W}$. The RMS current flowing through the siren will be $I_{RMS\ siren} = 13.6\text{V}/7.2\Omega = 1.89\text{A}$. The peak current flowing through the siren will be equal to $I_{peak\ siren} = \sqrt{2}I_{RMS\ siren} = 2.67\text{A}$. This is not so far beyond the rated power of the siren that it causes concern.

In our circuit, the siren is controlled by a MOSFET (Q1). When the MOSFET is not conducting, no current flows through the siren, and it is silent. On the other hand, when the MOSFET is conducting, its forward resistance is quite small, so that almost all of the voltage drop across the output terminals of the bridge rectifier is applied across the siren. We will need to select the MOSFET to be able to pass RMS and peak currents of 1.89A and 2.67A, respectively.

The sensors (S2 and S3)

Sensors S1 and S2 detect the presence of a magnetic field. Their internal resistance varies with the strength of the magnetic field. The resistance is not necessarily proportional to the distance which separates the sensor and its magnet, but it does not need to be. It is enough for our purposes that the sensor has a binary output voltage (or current) which indicates whether the magnetic field is present (door closed) or not (door open). It is for this reason that SPST magnetic reed switches could be used, although I used magnetic sensors for the four devices I have built.

As described above, the internal resistance of the sensors is 1.4KΩ when the magnet is close-by and 2.8KΩ when there is no magnetic field present. A 2KΩ fixed resistor (R1 and R2 in the schematic) is in series with each sensor. When the magnet is close-by, current equal to $I = V/R = 12V / 3.4K\Omega = 3.5mA$ will flow. When the magnet is removed, current equal to $I = V/R = 12V / 4.8K\Omega = 2.5mA$ will flow. It should be noted that the power consumed by R1 and R2 in the worst case will be equal to $P = I^2R = (3.5mA)^2 \times 2K\Omega = 24.5mW$. Quarter-watt resistors will easily suffice.

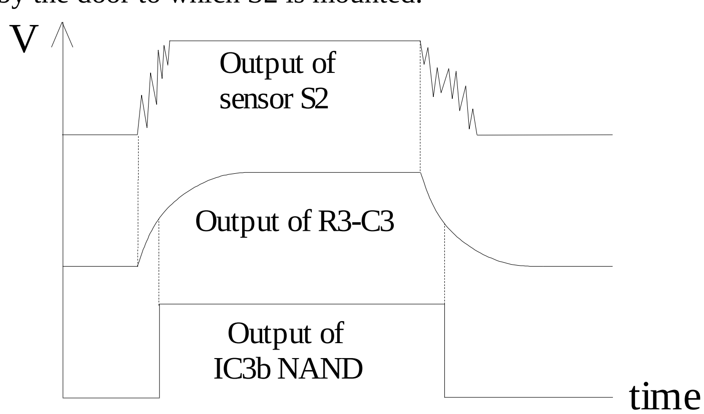
Cleaning up the sensor signal

It is best to clean up the sensors' output signals explicitly. This is done in our circuit by the R3-C3 and R4-C4 resistor-capacitor pairs. The two RC pairs are identical; one pair services the roll-up door sensor and the other services the man door sensor. Let me describe the R3-C3 pair, which process the signal from sensor S2. The voltage across capacitor C3 cannot change instantaneously. As described above, when the door is closed, the sensor voltage will be 4.9V. When the door is opened, the sensor voltage will jump to 7.0V. The voltage across C3 will increase from 4.9V to 7.0V only gradually, at a rate determined by resistor R3, which limits the amount of current flowing into capacitor C3. This rate is characterized by the R3-C3 time constant, which is equal to $\tau = R3 \times C3 = 100K\Omega \times 10\mu F = 1.0s$. The voltage over C3 will increase to the half-way voltage between its starting voltage (4.9V) and the applied voltage (7.0V) in 69% of one time constant, or 0.69s. This half-way voltage is (4.9V + 7.0V) / 2 = 5.95V. (It is noted as an aside that C3 actually charges up through the series combination of R1 and R3, a total of 102KΩ, and not simply through R3 at 100KΩ. The difference is negligible.)

This half-way voltage (5.95V) is important because it is at approximately this voltage (the mid-point of the 12V power supply) at which the hex inverter which follows in the circuit (IC2c, being one of the six inverters in a CD4069 chip) will change state. Roughly speaking, then, inverter IC2c will change state about seven-tenths of a second after the sensor first reports that the roll-up door has opened. This interval should be long enough for the magnet attached to the roll-up door to move well clear of the sensor. This will help to ensure that the on-off signals (noise) which will occur at the limit of the sensor's physical detection range will not cause phantom triggers.

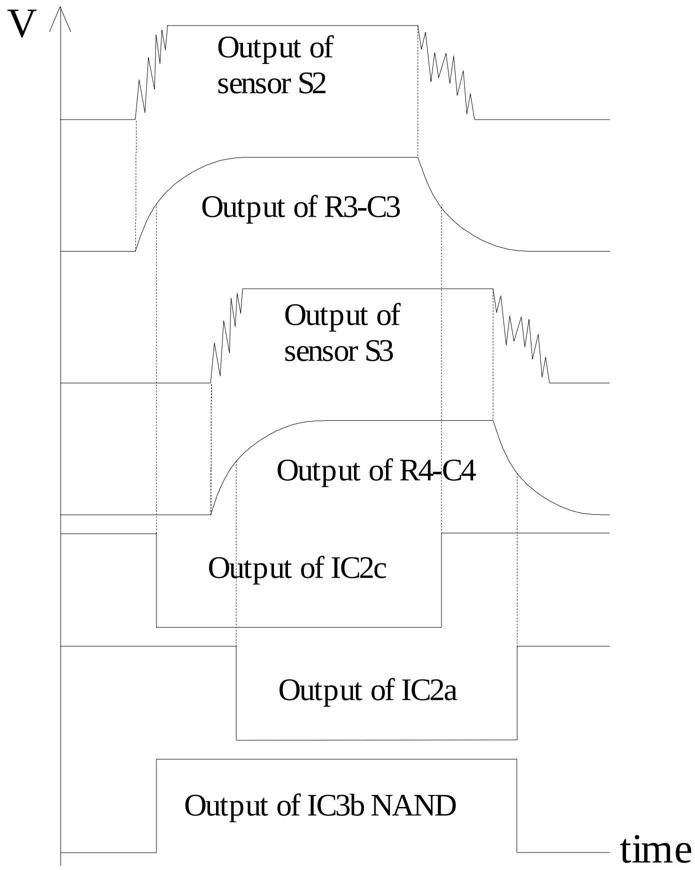
The output from inverter IC2c is one of the two inputs of the following gate, IC3b, which is one of the four NAND gates in a CD4011 chip. When capacitor C3 charges up to half-way voltage, inverter IC2c will flip from high to low. As soon as IC2c's output goes low, the output of the IC3b NAND gate will go high. It will either go from low to high, or it will remain high, but the important point is that it will be high. It will be high notwithstanding the state of the other sensor (S3) which determines the voltage on the other input line to NAND gate IC3b.

The relationships between sensor S2's output signal, the output from the R3-C3 pair and the output from the IC3b NAND gate are shown in the following figure. For this figure, it is assumed that the door to which S3 is mounted is closed, so that the output from NAND gate IC3b is determined solely by the door to which S2 is mounted.



Conflict between sensors

We need to address the potential for conflict between the two sensor inputs. What happens, for example, if the second door is opened when the first door is already open? The answer is most readily seen pictorially. The following figure shows the important voltages when the second door (monitored by sensor S3) is opened while the first door (monitored by sensor S2) is already open, and is then left open while the first door is closed.



It is clear from this figure that the output of the IC3b NAND gate will go from low to high when either door is opened from a condition in which both doors are closed. The output will remain high until both doors are once again closed. In operation, this means that the two minute grace period starts when either door is opened and that the siren will begin to sound two minutes later unless both doors are closed.

Using the device to monitor one door only

If it is intended to operate the device to monitor only one door, then the signal from the missing sensor must be disabled. This is done by tying the return line from the missing sensor to ground, which can be implemented using a jumper wire on terminal strip J2 between the missing sensor's signal line and ground.

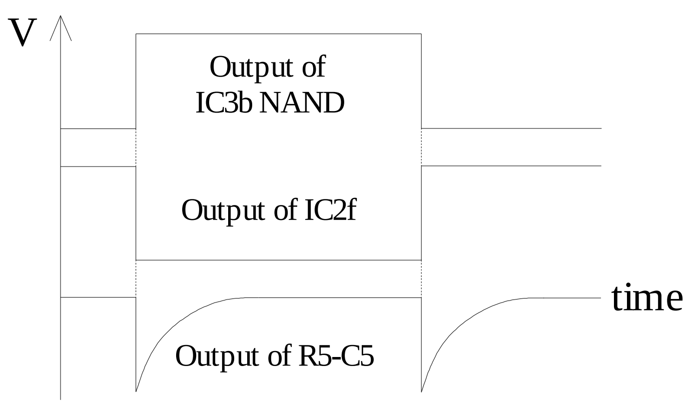
The timing circuit

The principal component in the timing circuit is an LM555 timer chip, IC4 (Digikey part # LM555CNFS-ND). It is wired as a "monostable", in which a single output pulse is generated by a change in voltage on the triggering input line. An external capacitor (C6) and an external resistor (R6) determine the duration of the output pulse. The values of these two components have been selected so that the output pulse is two minutes, or 120 seconds, long. C6 is constructed from two 68μF capacitors (Digikey part # 399-3597-ND) wired in parallel, giving a total capacitance of 136μF. They are tantalum capacitors, whose capacitance should change less with the passage of time than other types of capacitors. Resistor R6 is comprised of one 680KΩ metal film fixed resistor (R6A) in series with one 200KΩ trim potentiometer (R6B, Digikey part

490-2882-ND), giving a total resistance which can be varied linearly within the range from 680KΩ to 880KΩ.

The duration of the output pulse from IC4 is given by the formula $\Delta t = 1.1 \times R6 \times C6$. The duration will be in the range from a low of $1.1 \times 680K\Omega \times 136\mu F$, or 102s, to a high of $1.1 \times 880K\Omega \times 136\mu F$, or 132s. This should be a wide enough range to compensate for out-of-nominal component values or for the drift of component values with age. The trim potentiometer is adjusted until the observed duration of the output pulse is 120 seconds.

The output pulse from IC4 (on pin 3) is triggered by a falling edge on its input line (pin 2). The output from NAND gate IC3b could easily be inverted to provide such a falling edge, but that by itself is not enough. When using the LM555 chip, it is necessary that the triggering pulse be shorter than the output pulse. If the input line remains low when the output pulse ends, the 555 will re-trigger. This is prevented by using introducing another resistor-capacitor pair, R5 and C5, to process the output from IC3b. The pair is configured so that the rising voltage from IC3b, which is inverted by gate IC2f, is transmitted to pin 3 of IC4 without delay, but that resistor R5 thereafter recharges capacitor C6, returning the voltage at pin 3 to 12V regardless of the state of the output from IC3b. We want this recharge to take place fairly quickly. The time constant of the R5-C5 pair is equal to $\tau = R5 \times C5 = 10K\Omega \times 0.1\mu F = 1ms$. The relationships between the output from the IC3b NAND gate, the IC2f inverter, the R5-C6 pair and the triggering pulse are shown in the following figure.



Note that the LM555 is triggered on the falling edge of the R5-C5 voltage.

<u>Deriving the siren control signal</u>

Neither the triggering pulse (from pin 12 of IC2f) nor the output pulse (from pin 3 of IC4) have enough power to sound the siren. In fact, we do not even want the siren to sound during the two-minute duration of IC4's output pulse. We only want it to sound afterwards, and then to continue to sound until the roll-up door is closed. To combine the available signals in a useful way requires two more inverters and another NAND gate. When laying out the PCB, it was found convenient to use another NAND gate (IC3d), with its two input lines wired together, in place of an inverter.

NAND gate IC3a combines two signals. One of the two inputs to this NAND gate is the output from the IC3b NAND gate which, as we have already seen, is high when either or both doors are open. The output from the IC4 timer is inverted by IC2e and that signal delivered to the other input of NAND gate IC3a. IC3a's output line will therefore be low only if: (i) either door is open, so that the output from IC3b is high, and (ii) the output from the timer is low, meaning that the two-minute output pulse from IC4 has expired (or, if the doors were already closed, never happened). Under all other circumstances, IC3a's output will be low.

We invert this output using another inverter (NAND gate IC3d with the inputs tied together) and can use the resulting signal directly to control the gate of MOSFET Q1. This logic is summarized in the following truth table.

Condition of doors	Output from IC3b	Output from IC4	Output from IC2e	Output IC3a	Output from IC3d	Siren
Both closed	L	X	X	H	L	Off
At least one open less than 2 min.	H	H	L	H	L	Off
At least one open more than 2 min.	H	L	H	L	H	Sound

The MOSFET transistor

Q1 is an enhancement mode n-channel MOSFET. When its gate voltage is high (to be clarified), the transistor conducts. The MOSFET used (Digikey part # IRL3714ZPBF-ND) has a forward (drain-to-source) resistance of $R_{DS} = 16m\Omega$. This is negligible compared to the resistance of the siren which, as has been described, allows the flow of rectified alternating current of $1.89A_{RMS}$ with peak current of 2.67A when it sounds. The power which the MOSFET must dissipate in these circumstances is approximately $P = I^2R = (1.89A_{RMS})^2 \times 0.016\Omega = 57mW$. This is negligible power, and orders of magnitude less than the capability of the component.

We need to talk about the requirements for turning Q1 on. The datasheet for the MOSFET shows that it will conduct tens of amperes at a gate-to-source voltage of 4V or more. The pulses in our logic circuit, which occur at a voltage of 12V, have ample voltage for this purpose. Unlike a bipolar transistor, where the flow of current into or out of the base terminal "turns on" the transistor, a MOSFET is "turned on" by charging up the capacitance of its gate terminal. The rate at which charge is delivered to the gate determines how long it will be before the MOSFET's drain-to-source pathway begins to conduct. The basic question for us is whether gate IC3d, which drives the MOSFET's gate, can deliver enough charge to the gate capacitance of Q1 to turn it on quickly. Note first that IC3d drives the gate through 6.2KΩ resistor R7. This value of resistance was selected to avoid overpowering IC3d. The datasheet for the CD4011 shows that it has a maximum output current of 2.25mA at a supply voltage of 10V. R7 was selected so that the maximum current required from IC3d would always be less than 2.25mA. In the worst case, at the outset of charging the MOSFET's gate, the current through R7 is $I = V / R = 12V / 6.2K\Omega = 1.94mA$. This is well below the 2.25mA limit. But, how fast will R7 allow current to flow into the MOSFET's gate?

The datasheet for Q1 shows that its gate needs 4.8nC of charge to become active. Since this capacitance must charge up through R7, the time constant of the charge event is equal to $\tau = 6.2\text{K}\Omega \times 4.8\text{nC} = 29.8\mu\text{s}$. This is not particularly fast. In a high-speed repetitive switching application, this could cause problems because the MOSFET spends a fair bit of time in its transition mode. In our application, however, Q1 will be turned on only rarely (hopefully, never, if the roll-up door operators are conscientious). Furthermore, 29.8µs is instantaneous from the point-of-view of a human being so this delay in turning on the siren will not be noticeable.

Zener diode (D2) is a common 18V zener diode. It is placed across the gate-to-source junction of Q1 to prevent stray voltage spikes from damaging the gate. The datasheet for Q1 gives a maximum gate-to-source voltage of 20V. Zener diode D2 should clip otherwise-damaging spikes.

The LED indicators

There are four LEDs in our circuit. They make it easier to adjust the unit, so it can be done without the noise of the siren. They also allow the unit to be monitored from afar once it is installed.

LED1 indicates that the logic circuit is receiving power. It is biased by 2KΩ resistor R8 which limits the current flow. Assuming a 2V voltage drop over the LED when it is on, the current flowing through the resistor and the LED will be equal to $I = V/R = (12\text{V} - 2\text{V})/2\text{K}\Omega = 5\text{mA}$. LED1 is called the "Power On" indicator and is labeled with a "P" on the front panel.

LED2 is illuminated whenever either or both doors are open. It is a "Door Open" indicator. It is biased by 1KΩ resistor R8 which limits the current flow to 10mA. Note that the "Power On" LED was biased with a bigger resistor so that it consumes less power because it is, well, always on. LED2 and the two other LEDs are illuminated relatively infrequently so their power consumption is less of an issue. LED2 is labeled with an "O", for open.

LED3 is wired to the output line of the IC4 timer. It is illuminated during any two minute grace period. It is the "Two Minute" indicator and labeled with a "T" on the front panel.

LED4 responds to the signal applied to the MOSFET's gate. It is illuminated whenever the MOSFET is conducting and the siren is sounding. It is illuminated even if the siren is not connected. This LED is the "Siren" indicator and is labeled with an "S". LED3 and LED4 are biased to permit 10mA of current flow when illuminated.

I labeled these LEDs with single letters on the front panel of the enclosure. I did not want to provide the door operators with any more tools than necessary which might help them disable or circumvent the devices.

Terminal strips

Connectors J1 and J3 are two-screw terminal strips with 0.2" spacing, for convenience in hooking-up the power supply input and the siren output, respectively. Connector J3 and a similar connector used in construction to hook up the LEDs, but not shown in the schematic diagram, are six-screw terminal strips with 0.2" spacing, for use in hooking up signal wires.

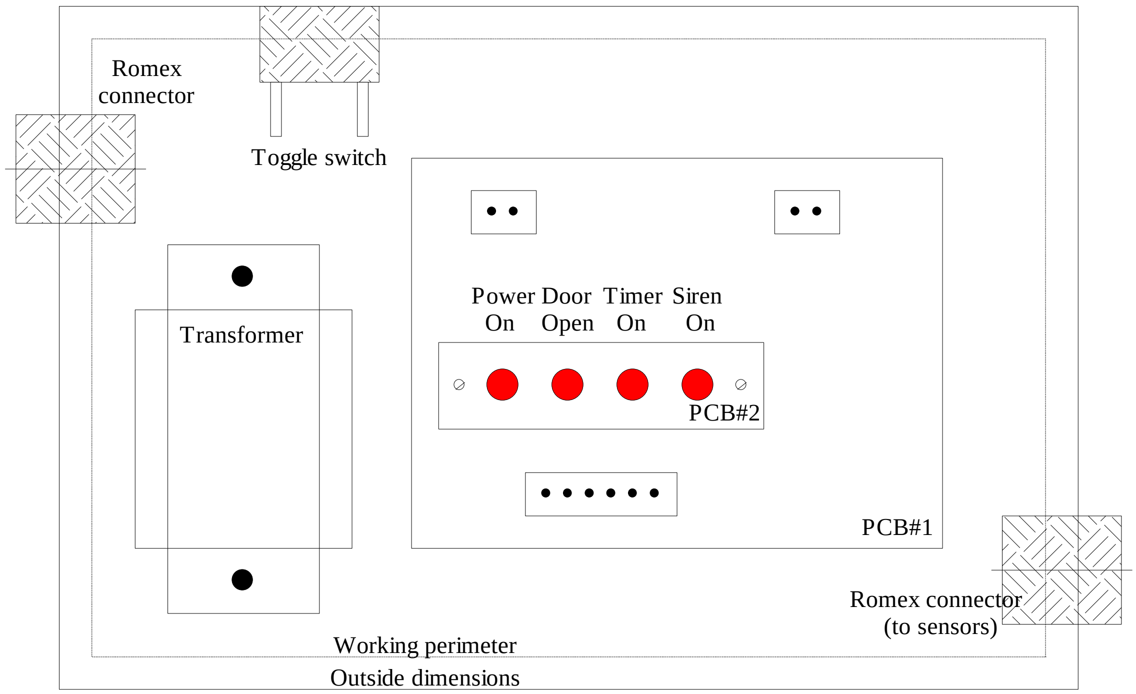
Wiring for other types of sensors

The sensors shown in the schematic diagram are normally-closed magnetic switch sensors. It should be clear that these sensors could be replaced with normally-closed SPST reed switches without any change.

It should be noted that the 2KΩ resistors R1 and R2 are shown in the schematic as being on the "outside" of terminal strip J2. In construction, these resistors were simply wired in between the appropriate screw positions on that terminal strip. Keeping resistors R1 and R2 off the printed circuit board allows easy conversion from the use of normally-closed sensors to the use of normally-open sensors.

The wiring configuration for the use of normally-open sensors is shown in a separate box in the upper-middle of the schematic diagram. All that is required is that the sensor and 2KΩ resistor be wired in such a way that the voltage labeled "Signal" goes from low-to-high when the magnet is withdrawn from the sensor.

The following figure is an outline drawing of the inside of the enclosure, looking through from front to back.



On the left side is the Romex connector which, when tightened up, secures the electrician's utility box to the enclosure. A similar Romex connector at the lower right is the egress point for the two pairs of wires to the sensors. The transformer is at the lower left and the SPST toggle switch for power on/off is at the top. Printed circuit board #1 (PCB#1) occupies the remaining area of the enclosure.

The small printed circuit board which holds the four LEDs (PCB#2) is bolted to the front face of the enclosure, with holes drilled through the face to allow the LED's to slide through.

The following photograph shows a finished unit, with the front panel unscrewed and placed far enough away from its normal position to allow the interior of the enclosure to be seen.

Jim Hawley
September 2013

An e-mail setting out errors and omissions would be appreciated.

In response to readers' questions:

1. Resistors R1 and R2 are not mounted on either printed circuit board. They are wired across the appropriate screws on terminal strip J2. This gives the user some flexibility in two circumstances. Firstly, the difference between the open and closed resistances of the sensors can differ from manufacturer to manufacturer. The objective is to set the value of the bias resistors, that is, R1 and R2, to the mid-point of the open and closed resistances.

This will cause the input voltages to inverters IC2a and IC2c to bracket 6V, which is roughly its switching point. Secondly, keeping R1 and R2 off the PCB makes it a lot easier to reconfigure things for normally-open sensors.

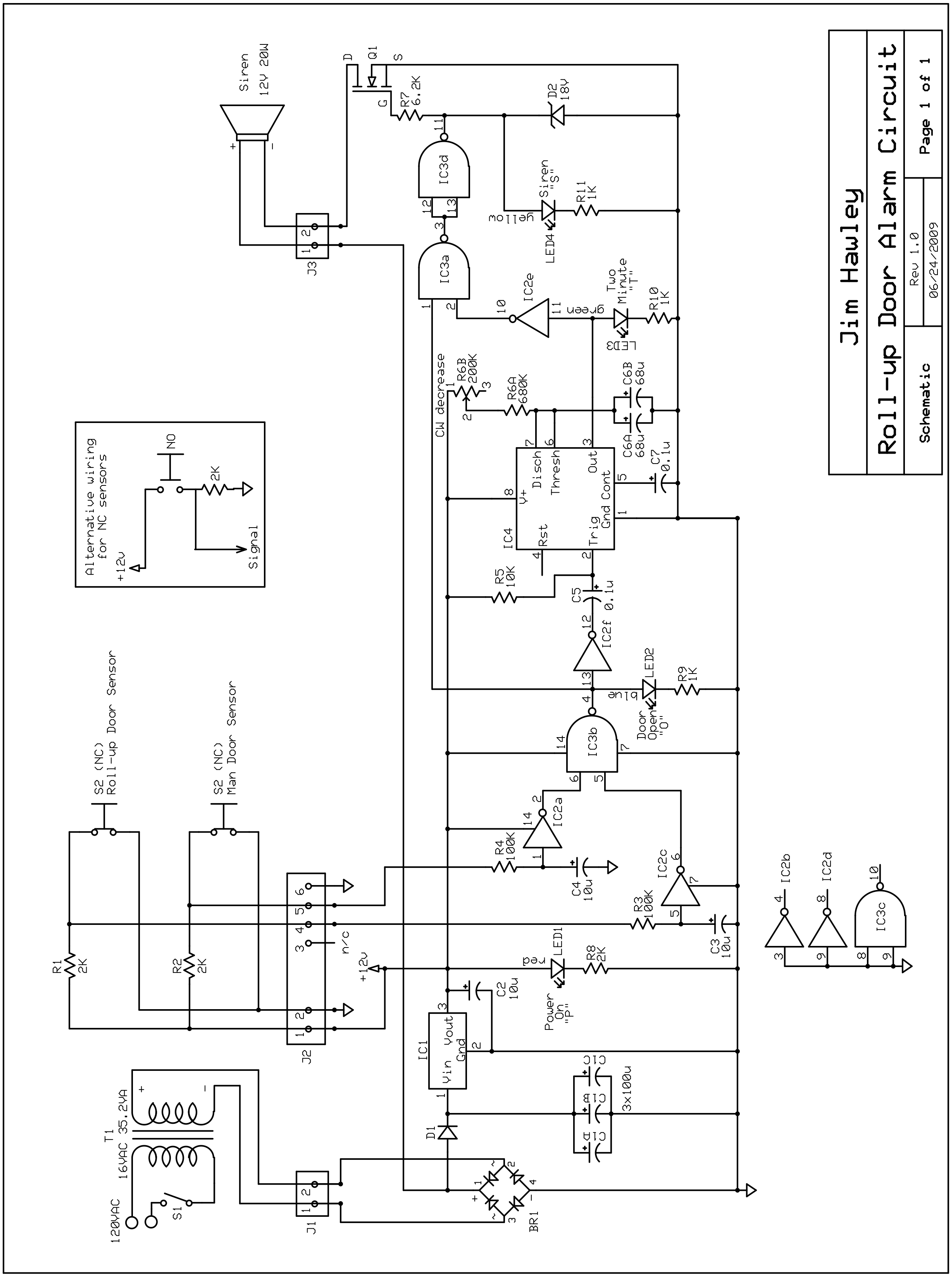
2. On the schematic diagram, the anodes of the four LEDs are labeled with the colours red, blue, green and yellow. These are the colours of the insulation on the hook-up wires from PCB#2, which is bolted to the front panel, to the terminal strip on PCB#1. This is a matter of convenience only.

3. I have used “normally-open” and “normally-closed” to describe the state of the internal <u>switch</u> of the sensor when the magnet piece is face-to-face with the sensor piece. The state of the switch is not the same thing as the state of the <u>door</u>, which can of course be open or closed.

4. I prefer normally-closed sensors because current flows through the sensor in the “normal” position, which I want to be a closed door. It happens that, in this configuration, the switch and the door are both “open” or “closed” together. Having current flow through the sensor in the “normal” position means that any disruption to the circuit, such as a wire being cut, will cause the siren to sound.

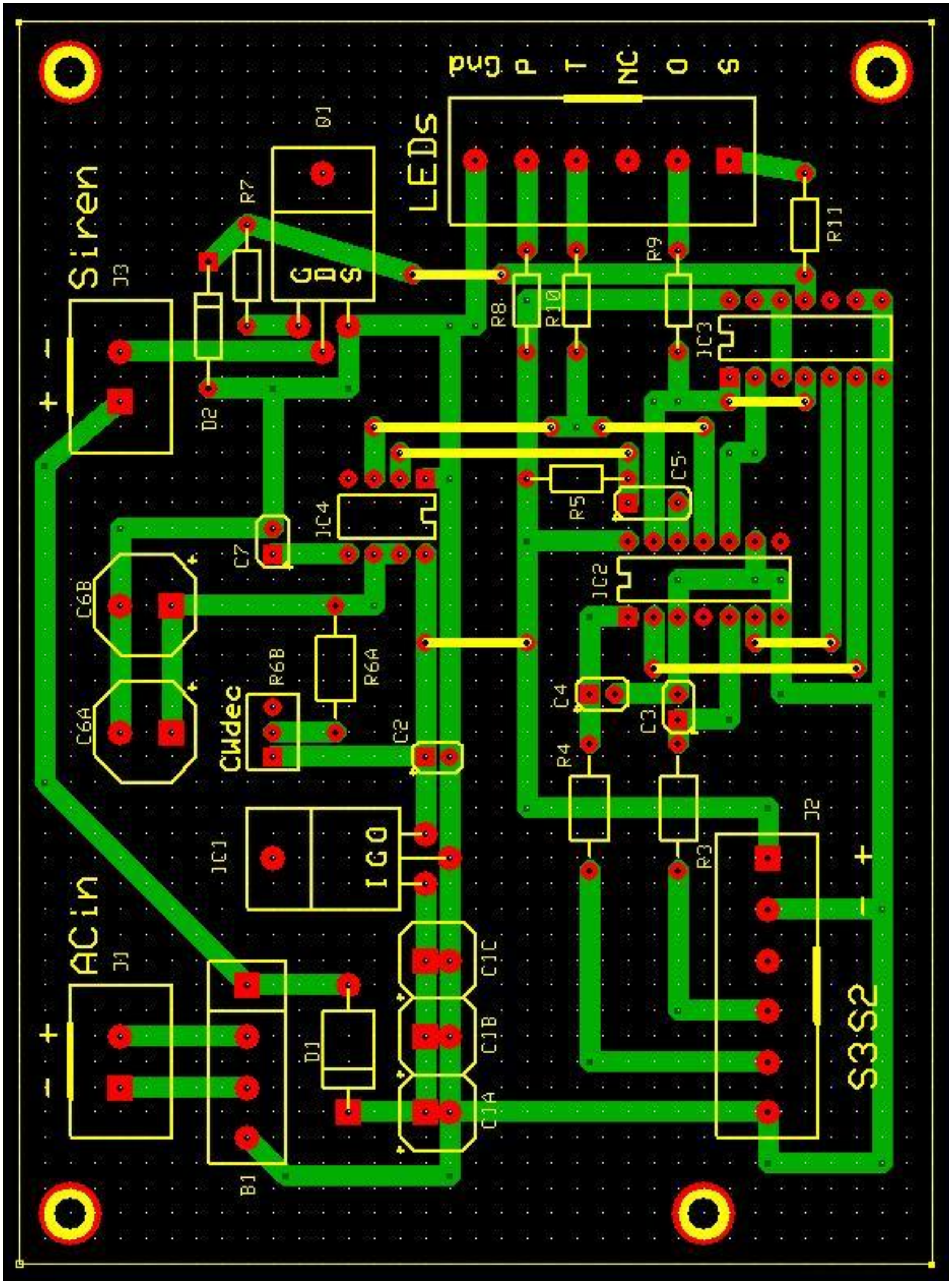
Appendix "A"

<u>Schematic diagram</u>



Appendix "B"

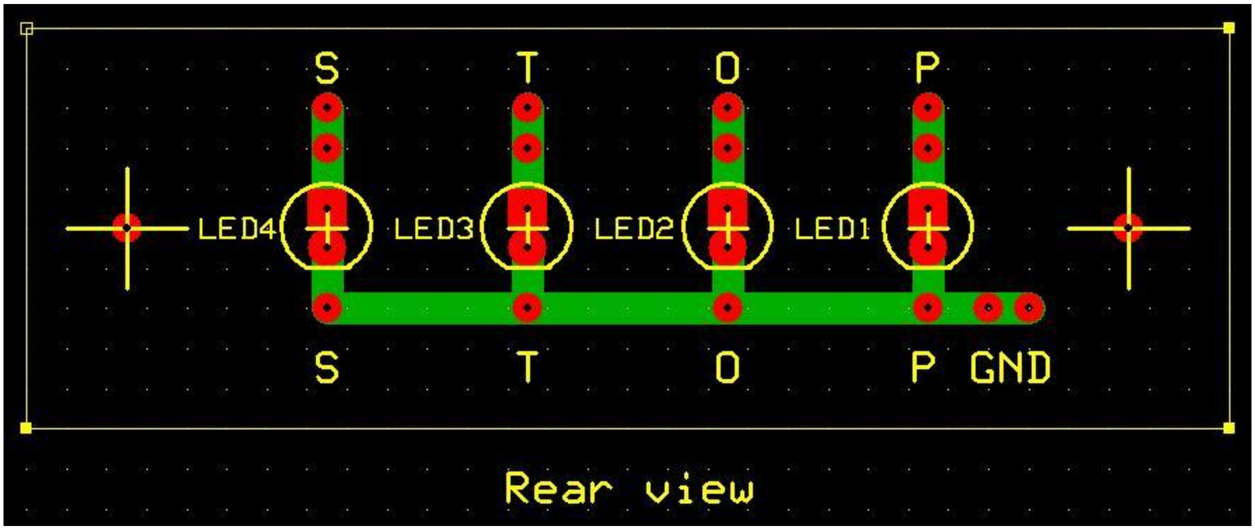
Printed circuit board PCB #1, for the logic circuit
(Board dimensions: 4.90 inches wide by 3.60 inches high)



Appendix "C"

<u>Printed circuit board PCB #2, to hold the indicator LEDs</u>

(Board dimensions: 3.00 inches wide by 1.00 inch high)



Appendix “D”

Bill of materials

BILL OF MATERIALS

Name	**Circuit symbol**	**Digikey part no.**	**Description**
Toggle switch	S1	360-1896-ND	15A at 125VAC, SPST, solder lug
Transformer	T1	HM533-ND	16VAC at 2.2A, 35.2VA
Bridge rectifier	BR1	RS403GL-BPMS-ND	4A, 200VAC PIV, 4-lead in line
Blocking diode	D1	1N5402DICT-ND	1V at 3A, 200PIV
Voltage regulator	IC1	497-1464-5-ND	+12V, 500mA, TO-220
Hex Inverter	IC2	296-3518-5-ND	3-15V, 2.25mA, 14-DIP (CD4069)
NAND gate	IC3	296-2031-5-ND	3-15V, 2.25mA, 14-DIP (CD4011)
555 Timer	IC4	LM555CNFS-ND	4.5-16V, 15mA, 8-DIP
MOSFET	Q1	IRL3714ZPBF-ND	36A, 20V, 16mOhm, TO-220
Zener diode	D2	1N4746ADICT-ND	18V, 1W, 5%
LEDs	LED1-LED4	160-1701-ND	5mm, red transparent, 90mcd, 2V
Filter capacitors	C1A,C1B,C1C	565-1059-ND	100uF, 25V, 20%, electrolytic
10uF capacitors	C2,C3,C4	478-1839-ND	10uF, 16V, 10%, tantalum
0.1uF capacitors	C5,C7	478-1831-ND	0.1uF, 35V, 10%, tantalum
68uF capacitor	C6A-B	478-1926-ND	68uF, 16V, 10%, tantalum
1K resistors	R9-R11	P1.00KCACT-ND	1.00K, 1/4W, 1% metal film
2K resistors	R1,R2,R8	2.00KXBK-ND	2.00K, 1/4W, 1% metal film
6.2K resistor	R7	S6.2KCACT-ND	6.20K, 1/4W, 1% metal film
10K resistor	R5	P10.0KCACT-ND	10.0K, 1/4W, 1% metal film
100K resistors	R3,R4	P100KCACT-ND	100K, 1/4W, 1% metal film
680K resistor	R6A	P680KCACT-ND	680K, 1/4W, 1% metal film
Potentiometer	R6B	490-2882-ND	200K, 25 turn, linear, top adj.
Enclosure	-	HM930-ND	9.4"x6.3"x3.5", ABS, flat top
Siren	Siren	-	12VDC 20W