A triggering circuit for the high-power SCR in a coil gun

A silicon-controlled rectifier ("SCR") in a circuit is a lot like a diode. It allows current to flow in one direction, but not the other. Unlike a diode, though, an SCR has a third terminal, its "gate". The voltage applied to the gate determines when the SCR will permit conduction to start. Even if the main current channel through the SCR is forward-biased, the SCR will not allow current to begin flowing unless and until the voltage applied to the gate is raised above a certain threshold. Once current begins to flow through the main channel, the SCR will permit it to continue to flow even if the voltage applied to the gate is removed. Conduction will stop only when the main channel becomes reverse-biased.

For small SCR's, the subcircuit which controls the gate voltage can be pretty simple. For higher power SCR's, the control subcircuit must be able to deliver a relatively large current into the gate, while maintaining the voltage above the threshold at the same time. There is a reason for this. As SCR's get larger, the effective capacitance of their internal gate circuitry becomes larger. It is not enough to simply "apply a voltage". The designer must understand that the gate is really a capacitor, and the voltage drop over the gate can only rise as current flows into that capacitance and charges it up.

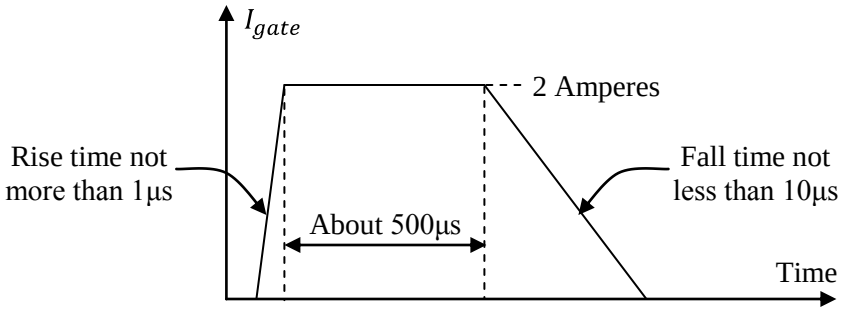
For very high power SCR's, the requirements for the gate subcircuit become even more demanding. There is a reason for this, too. Thousands of Amperes of current cannot flow through a pinhead. The active cross-sectional area of a high-power SCR is physically big. Think in terms of a hefty fraction of a square inch. In order for the SCR to "turn on" and begin conducting like a diode, the entire physical surface needs to become forward-biased. Large SCR's usually have internal circuitry, called amplifiers, whose purpose is to distribute the current flowing into the gate across the entire cross-sectional area in an attempt to "turn on" as much area as possible in as short a time as possible.

Datasheets for high-power SCR's contain very specific recommendations about the voltage and current waveforms which the gate control subcircuit should deliver. The purpose of this paper is to think through such a subcircuit.

In an earlier paper titled *Using FEMM to simulate the firing of a coil gun*, I simulated a coil gun powered by a 16,000μF capacitor charged initially to 390 Volts. The current which flowed through the circuit reached a high of about 3,000 Amperes.

I have looked through the SCR's available from www.DigiKey.com to find ones which are in this ballpark. I have settled on DigiKey's part number VS-ST230C12C0GI-ND. This is an SCR made by Vishay. It can pass 410 Amperes of continuous d.c. current, but a much higher 60Hz alternating current – up to 7,000 Amperes. On the assumption that the coil gun is fired intermittently, and has a chance to cool down between firings, this SCR is a contender. It is the one I will use in the following numerical example. This SCR has a reverse-blocking voltage of 1,200 Volts, which is higher than we need, but DigiKey does not carry in stock lower voltage SCR's in this series.

The current waveform I would like to apply to the SCR's gate is the following:



In order to explain why I want this waveform, I have to make reference to some of the parameters set out in the SCR's datasheet. For ready reference, I have copied Vishay's SC230C into Appendix "A". I hope they don't mind. ("Buy Vishay's stuff." There, that should do it.)

A good rule-of-thumb to use with SCR's is: "turn them on hard and fast". I would like the turn-on current to be 2 Amperes, which is a goodly fraction of the "Maximum peak positive gate current" ($I_{GM} = 3\text{A}$) which will fry the device.

The rise time should be as fast as possible. The rise time is closely related to the "Typical delay time" ($t_d = 1.0\mu s$) given in the datasheet. The circuit which drives the gate should, at a minimum, be faster than this.

On the other hand, the fall time should not be too fast. In some instances, a very rapid fall of the gate voltage can trick the SCR into turning itself off. We do not want that to happen. The datasheet does not give a figure to say how fast is too fast, but it does give a "Typical turn off time" ($t_q = 100\mu\text{s}$). This is the time it takes a typical device to turn itself off after the current through the main channel goes negative. Based on that figure, I will try to arrange the driving subcircuit so that the current it delivers falls on a time-scale of 10μs.

How long do we want the current pulse to last? This is an important question. In theory, SCR's will continue to conduct, whether the gate current is removed or not, once a certain amount of current starts to flow through the main channel. The datasheet reports two values which are related to this. They are the "Maximum holding current" ($I_H = 600\text{mA}$) and the "Maximum latching current" ($I_L = 1A$). The latter figure (1A) is the amount of current flowing through the main channel which will cause the device to latch into its conduction mode, after which the gate current can be removed. The former figure (600mA) is the amount of current which must continue to flow through the main channel, below which it will begin to close. The currents we experience in our coil gun circuit are many, many times bigger than this. A close examination of the rise and fall of the current in an earlier paper titled *Using FEMM to simulate the firing of a coil gun* shows that the current flowing in the main circuit will be greater than one Ampere in less than one microsecond, if all components work as we would like. That means that the duration of the current pulse which the gate-driver subcircuit has to apply could be as short as just a few microseconds. Longer is better, though, since it ensures a good, clean, fast turn-on.

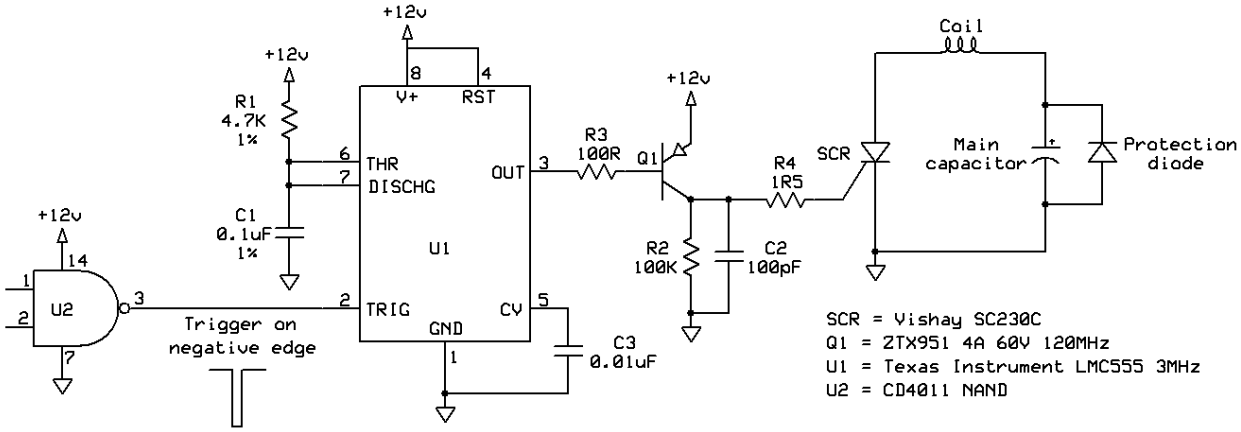
But, we do not want the gate-driver current to last too long. The principal issue here is that we could find ourselves in a position where the current through the main channel current has fallen to zero, or below, while the gate current is still flowing. The SCR will still function in the proper manner, by turning off to block negative current flow, but the leakage current will be much higher than usual if the gate is still forward-biased when the main channel is reverse-biased. The circuit we looked at in the earlier paper had a current pulse which was a total of about two milliseconds long, with the peak current experienced about half-way through, at one millisecond.

I think a good compromise is to allow the gate-driver to deliver a pulse about one-half millisecond long, so it will last about one-quarter of the duration of the entire main channel pulse.

Let me mention two other figures which are given in the datasheet. The first one is the "Maximum non-repetitive rate of rise of the turned-on current" ($dI/dt < 1{,}000\ \text{A}/\mu\text{s}$). This relates to the current flowing in the main channel, not to the current delivered by the gate-driver subcircuit. It puts a limit on the rate at which the current flowing through the main channel can be permitted to rise. Our coil gun circuit is well below that threshold, by a factor of several hundred. It takes about one millisecond for the primary current to reach approximately 3,000 A, which is a rate of about $3\ \text{A}/\mu\text{s}$. The second limiting figure is

the "maximum critical rate of off-state voltage" ($dV/dt < 500\ \text{V}/\mu\text{s}$). This figure, too, relates to the main channel. If the forward-baised voltage across the main channel of the SCR rises too quickly, the device can be tricked into turning itself <u>on</u>, even if the gate voltage / current are still held low. We do not want the phenomenon to cause a false trigger. In our application, this restriction means that we should not charge up the principal capacitors at a faster rate than this. That is unlikely in any event – changing a 16,000µF capacitor up to 390 Volts is going to take a lot longer than one microsecond.

A schematic of the circuit I propose to trigger the SCR is the following.



The duration of the current pulse is controlled by a 555 timer chip configured as a monostable (generating only one output pulse). A negative-going voltage edge on the input pin 2 causes a positive pulse to be generated on the output pin 3. The duration of the pulse is determined by two external components, being the 4.7K resistor R1 and the 0.1µF capacitor C1. The exact duration of the pulse is given by the following formula:

$$\begin{aligned}\text{Duration} &= 1.1 \times \text{R1} \times \text{C1} \\ &= 1.1 \times 4.7\text{K} \times 0.1\mu \\ &= 517\mu\text{s}\end{aligned}$$

This is close enough to the desired one-half millisecond for our purpose. Even so, I have specified $\pm 1\%$ tolerances so that the duration does not get too far afield.

The 555 timer chip I am proposing to use is Texas Instruments' LMC555, which DigiKey sells as its part number LMC555CN/NOPB-ND. I have selected this chip because it is relatively fast as 555 timer chips go. It is rated for a cycle time of 3MHz when operated in astable mode, generating a series of pulses. If it can produce a complete pulse in a time of 1 / 3MHz = 0.33µs, then we can be sure that its rise and fall times are much shorter than that. Furthermore, its output pin can deliver up to 50 mA of current with which to drive the transistor Q1 which follows it in the circuit.

The 50 mA which the 555 timer chip can deliver is not enough to drive the SCR's gate. Transistor Q1 amplifies the current to the level we need. I am proposing to use DigiKey's part number ZTX951-ND, which is a pnp transistor made by Diodes Incorporated. I selected this one for a couple of reasons. It is rated for a collector-emitter current of 4A (twice what we need), is rated for a collector-emitter voltage of 60V (five times greater than the 12V logic power supply voltage) and is rated for frequencies up to 120MHz (much faster than the 555 timer chip).

Transistor Q1 plays the role of a switch in the circuit. Other than during the short periods of time when it is changing state, Q1 will be either fully turned-on (operating in its saturation mode) or entirely turned-off (operating in its cut-off mode). When the voltage on Q1's base is high, Q1 will be in saturation mode and the voltage at its emitter will be approximately 12 Volts. When the voltage on Q1's base is low, it will be cut-off and the voltage at its emitter terminal will also be low. Q1's emitter terminal is tied to the SCR's gate by a very small resistor so the voltage of the SCR's gate will track the voltage on Q1's emitter quite closely. Let me describe the details.

When Q1 operates in its saturation mode

The datasheet for the ZTX951 states that its (minimum for any device) d.c. current gain (h_{FE}) is in the range of 75 to 100 when collector currents are in the 1A to 4A range. The d.c. current gain is the ratio of the collector-to-emitter current divided by the current flowing into the base. Just to pick a representative number, let me use $h_{FE} = 87.5$ at the design collector current of 2A. Then, the current flowing into the base will be:

$$I_B = \frac{I_C}{h_{FE}} = \frac{2A}{87.5} = 22.9\text{mA}$$

If this is the current flowing into the base, through base resistor R3 (100Ω), then the voltage drop over the base resistor will be:

$$V_{R3} = 22.9\text{mA} \times 100\Omega = 2.3 \text{ Volts}$$

The voltage at Q1's base terminal will be the voltage of the 555 timer chip's output pin (12 Volts) less the voltage drop over the base resistor:

$$V_B = 12 - 2.3 = 9.7 \text{ Volts}$$

The datasheet for the ZTX951 states that its collector-emitter voltage when in saturation is in the range 0.15 Volts to 0.25 Volts, depending on the collector current. Using 0.2 Volts as an average, we can calculate that the voltage on Q1's emitter terminal will be as follows:

$$\begin{aligned} V_E &= V_C - V_{CE,sat} \\ &= 12 - 0.2 = 11.8 \text{ Volts} \end{aligned}$$

In order to operate in saturation mode, the voltage on Q1' s n-doped terminal (the base) needs to be less than the voltage on both of its p-doped terminals (both the collector and emitter). That is the case, confirming that Q1 is operating in saturation mode. Both of its p-n junctions, from the collector to the base and from the emitter to the base, are forward-biased.

Let's look at the current flowing into the SCR's gate next. The following figure is a graph extracted from the datasheet. It shows the voltage-versus-current characteristics of the gate. I will try to bias the gate-driver subcircuit so that it operates at the point shown by the red dot in the graph. At this particular point, the voltage drop over the gate is $10V$ and the current flowing into the gate is $1A$.

In the driver subcircuit, the current flowing into the gate (I_G) flows through resistor R4. The voltage drop over the resistor will be $V_{R4} = \text{R4} \times I_G$. The voltage at the SCR's gate (V_G) will be the voltage at Q1's emitter less this voltage drop. That is:

$$V_G = V_E - V_{R4} = 11.8 - (\text{R4} \times I_G)$$

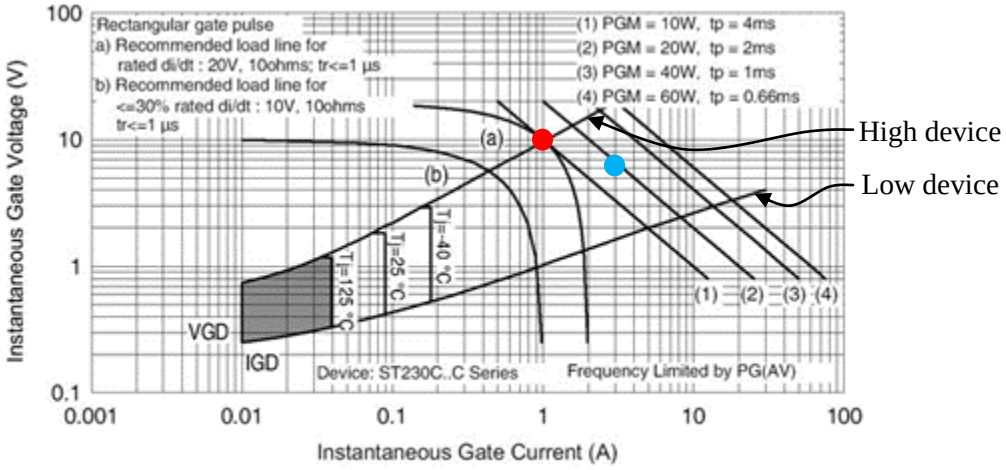


Fig. 11 - Gate Characteristics

At the design operating point ($V_G = 10V$ and $I_G = 1A$), this expression reduces to:

$$V_G = 11.8 - (\text{R4} \times I_G)$$
$$\rightarrow \quad \text{R4} = \frac{11.8 - V_G}{I_G} = \frac{11.8 - 10}{1} = 1.8\Omega$$

Now, there are two principal curves from the lower left to the upper right) in the graph of the SCR's gate characteristics. They represent the extremes found in the devices. The red dot I selected for the operating point is for the "high device". In a sense, this represents a device with a high gate voltage and low gate current, in other words, high gate resistance. What if the device has a lower gate resistance? Suppose its gate accepts 3A of current when the gate resistor is set to 1.8Ω. Then, the gate voltage will be:

$$V_G = 11.8 - (1.8 \times 3) = 6.4 \text{ Volts}$$

I have placed a blue dot at this co-ordinate ($I_G = 3, V_G = 6.4$) in the characteristic graph. This point falls underneath line (2) in the graph, which marks the maximum values permitted for pulses which are two milliseconds long. Since we will be using a pulse length of one-half millisecond, we should be OK.

Let me talk about the effect of resistor R2 and capacitor C2 when transistor Q1 is first turned on. Part of the current which starts to flow through Q1's collector circuit will be used to charge C2 up to the emitter voltage $V_E = 11.1$ Volts. Since our goal is to pump current into the SCR's gate as fast as possible, the diversion of current into C2 is unwelcome. I have minimized the impact of the diversion by making C2 a very small capacitor, only 100pF. It needs only $\Delta Q = \text{C2} \times V_E = 100 \times 10^{-12} \times 11.1 = 1.1 \times 10^{-9}$ Coulombs of charge to reach the emitter voltage. This much charge can be delivered by 1A of current in 1.1 nanoseconds. This is only 0.1% of the one microsecond in which we hope to turn on the SCR, so the diversion of charge is very minor.

<u>When Q1 is cut-off</u>

I have placed resistor R2 and capacitor C2 in the circuit to deal with the circumstance when transistor Q1 is turned off. This will occur when the positive pulse from the 555 timer chip comes to an end. The

voltage on Q1's base will drop to ground quite quickly. C2 will remain changed up, at least for a short moment, so Q1's base-to-emitter junction will be reverse-biased. Q1 will be cut off and current will stop flowing through the collector-to-emitter pathway. This will leave the R2-C2 pair as a passive loose end. The voltage over capacitor C2 will decay as the current flows out of C2 and through R2 to ground. The time-constant of this decay will be $\tau = \mathrm{R2} \times \mathrm{C2} = 100\mathrm{K} \times 100\mathrm{p} = 10^5 \times 10^{-10} = 10\mu\mathrm{s}$. It will take about five time constants, or 50 microseconds, for the voltage at the SCR's gate to decay to zero. The purpose of R2 and C2 is to prevent too fast a decline in the gate voltage, which could trick the SCR into turning itself off.

The purpose of U2

The 555 timer is triggered by a falling edge. U2 is a 2-input NAND gate which produces a short pulse whose second edge is the triggering event. I have not specified what its two inputs are. I will do so in subsequent papers. It is enough for now to say that one of the inputs will be a "safety" voltage, which will only be high when everything is ready for firing the coil gun: the capacitors are charged, the position and speed sensors are clear, and so on. The second input is the positive-going trigger pulse for this particular coil in the gun. A button pressed by the user will be sufficient for the first coil. But, if the gun has multiple coils, the triggering circuits for the second and later coils can be based on either timers or detectors. In any event, the output of U2 will go low only if and when both input lines are high.

Jim Hawley

If you found this description helpful, please let me know. If you spot any errors or omissions, please send an e-mail. Thank you.

Appendix "A

Copy of the Vishay 230C datasheet

Phase Control Thyristors (Hockey PUK Version), 410 A

TO-200AB (A-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free RoHS COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
Package	TO-200AB (A-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	410 A
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V, 1400 V, 1600 V, 1800 V, 2000 V
V_{TM}	1.69 V
I_{GT}	90 mA
T_J	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		410	A
	T_{hs}	55	°C
$I_{T(RMS)}$		780	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	5700	A
	60 Hz	5970	
I^2t	50 Hz	163	kA^2s
	60 Hz	149	
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	Typical	100	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST230C..C	04	400	500	30
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			410 (165)	A
					55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled			780	A
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	5700	
		t = 8.3 ms			5970	
		t = 10 ms	100 % V_{RRM} reapplied		4800	
		t = 8.3 ms			5000	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		163	kA^2s
		t = 8.3 ms			148	
		t = 10 ms	100 % V_{RRM} reapplied		115	
		t = 8.3 ms			105	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			1630	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.92	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.98	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.88	mΩ
High level value of on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.81	
Maximum on-state voltage	V_{TM}	I_{pk} = 880 A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			1.69	V
Maximum holding current	I_H	T_J = 25 °C, anode supply 12 V resistive load			600	mA
Maximum (typical) latching current	I_L				1000 (300)	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ µs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/µs
Typical delay time	t_d	Gate current 1 A, dI_g/dt = 1 A/µs V_d = 0.67 % V_{DRM}, T_J = 25 °C	1.0	µs
Typical turn-off time	t_q	I_{TM} = 300 A, $T_J = T_J$ maximum, dI/dt = 20 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 Ω, t_p = 500 µs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10.0		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		2.0		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3.0		A
Maximum peak positive gate voltage	$+ V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	$- V_{GM}$			5.0		V
DC gate current required to trigger	I_{GT}	T_J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	180	-	mA
		T_J = 25 °C		90	150	mA
		T_J = 125 °C		40	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = - 40 °C		2.9	-	V
		T_J = 25 °C		1.8	3.0	V
		T_J = 125 °C		1.2	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	°C
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	K/W
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	K/W
		DC operation double side cooled	0.017	K/W
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-PUK)	

ΔR_{thJC} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.015	0.017	0.011	0.011	$T_J = T_J$ maximum	K/W
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.036		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

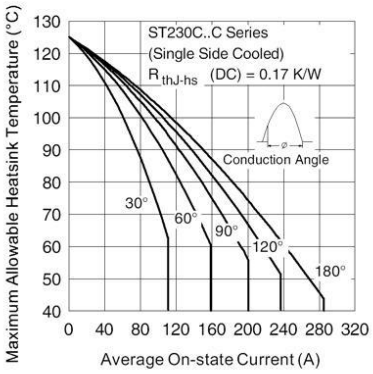


Fig. 1 - Current Ratings Characteristics

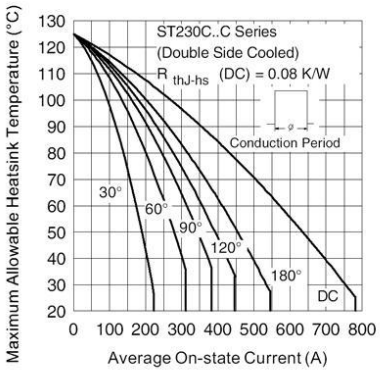


Fig. 4 - Current Ratings Characteristics

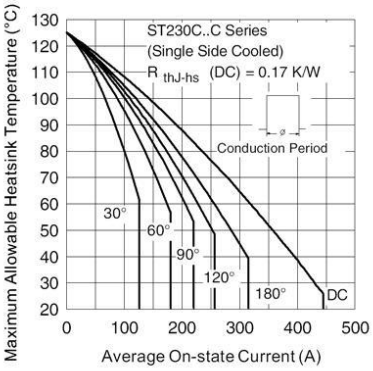


Fig. 2 - Current Ratings Characteristics

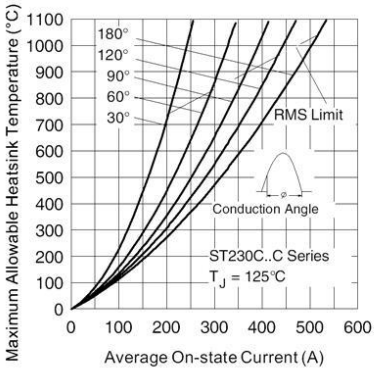


Fig. 5 - On-State Power Loss Characteristics

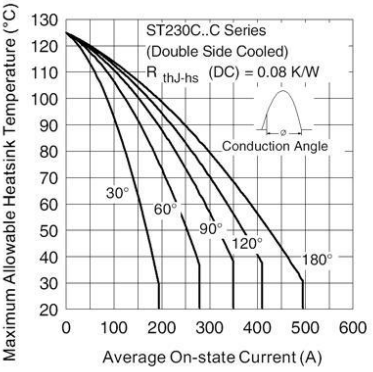


Fig. 3 - Current Ratings Characteristics

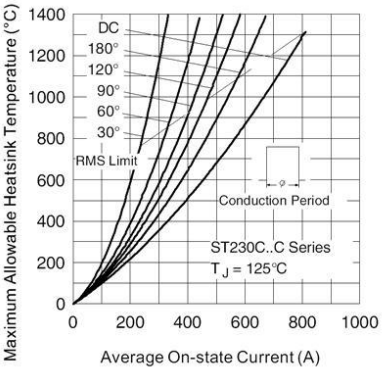


Fig. 6 - On-State Power Loss Characteristics

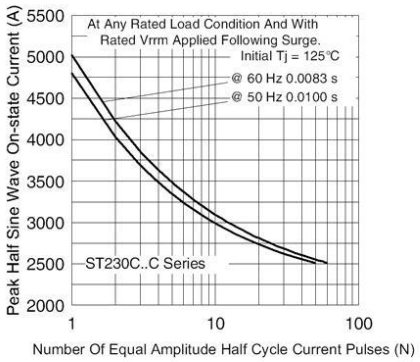


Fig. 7 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

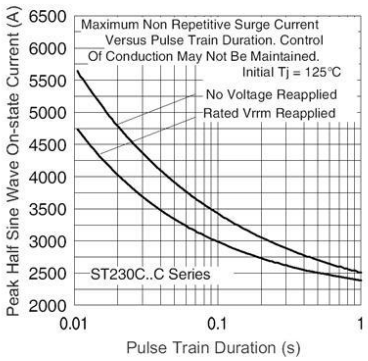


Fig. 8 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

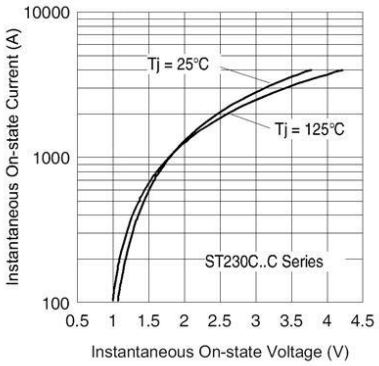


Fig. 9 - On-State Voltage Drop Characteristics

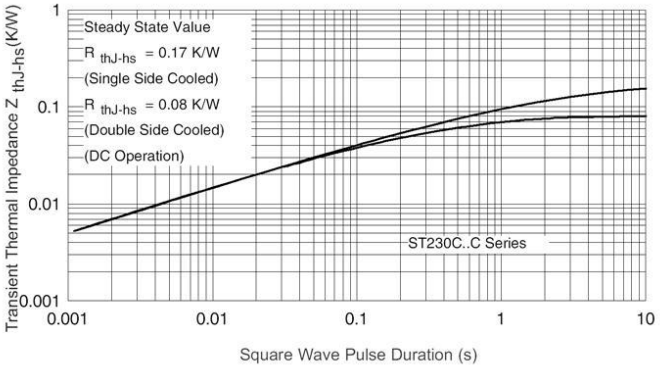


Fig. 10 - Thermal Impedance $Z_{thJ\text{-}hs}$ Characteristics

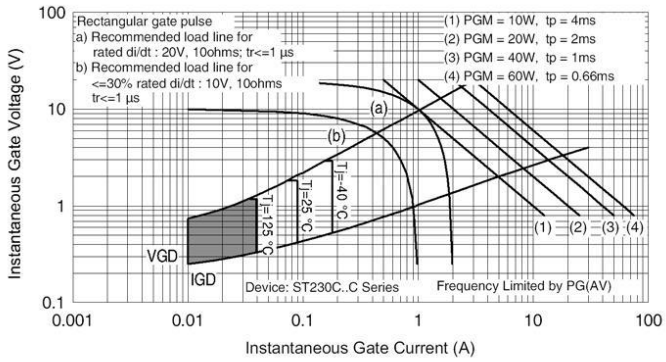


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

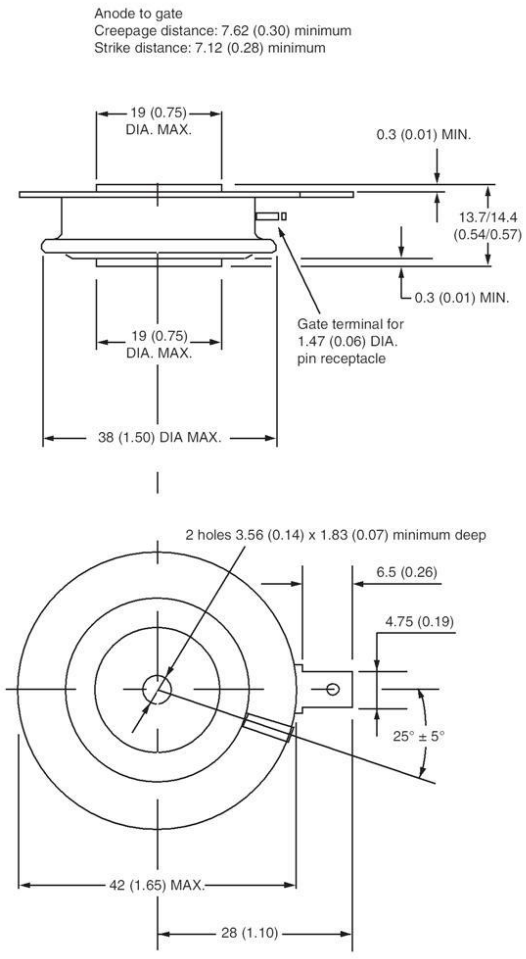
VS-	ST	23	0	C	20	C	1	-
1	2	3	4	5	6	7	8	9

1 - Vishay Semiconductors product
2 - Thyristor
3 - Essential part number
4 - 0 = Converter grade
5 - C = Ceramic PUK
6 - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
7 - C = PUK case TO-200AB (A-PUK)
8 - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
9 - Critical dV/dt: • None = 500 V/µs (Standard selection)
• L = 1000 V/µs (Special selection)

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95074

TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)

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