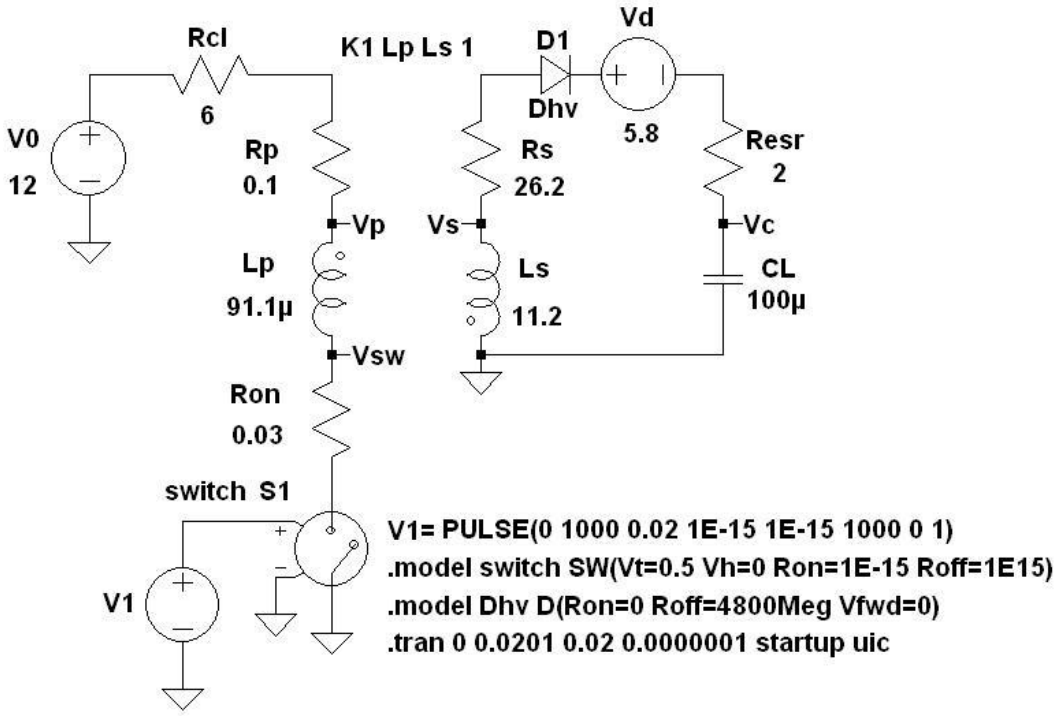
# A High-Voltage Buck-Boost Capacitor Charger

Reference is made to an associated paper titled *A High-Voltage Boost Capacitor Charger*. The earlier paper examined a capacitor charger in which the primary and secondary circuits worked in phase. In this paper, an alternative configuration will be examined, in which the primary and secondary circuits operate out of phase.

The following schematic diagram shows the principal components of the circuit. The component values shown are the same as used in the earlier paper, where details about their selection and construction can be found. The primary winding of the toroid transformer is represented by its ideal inductance $L_p$ and series resistance $R_p$. The secondary winding is represented by its ideal inductance $L_s$ and series resistance $R_s$. When conditions in the secondary circuit permit, diode $D_1$ conducts and the flow of current adds charge to the load capacitor $C_L$. Diode $D_1$ is represented by an ideal diode in series with a constant forward voltage drop of 5.8V. The load capacitor $C_L$ is represented by an ideal 100µF capacitor and an equivalent series resistance of $R_{esr}$. In the primary side, the current from the 12V dc power supply is limited by current-limiting resistor $R_{cl}$. The MOSFET which turns the primary circuit on and off is represented in this schematic by a simple SPST switch $S1$ which is accompanied in series by the MOSFET's ON-resistance $R_{on}$.

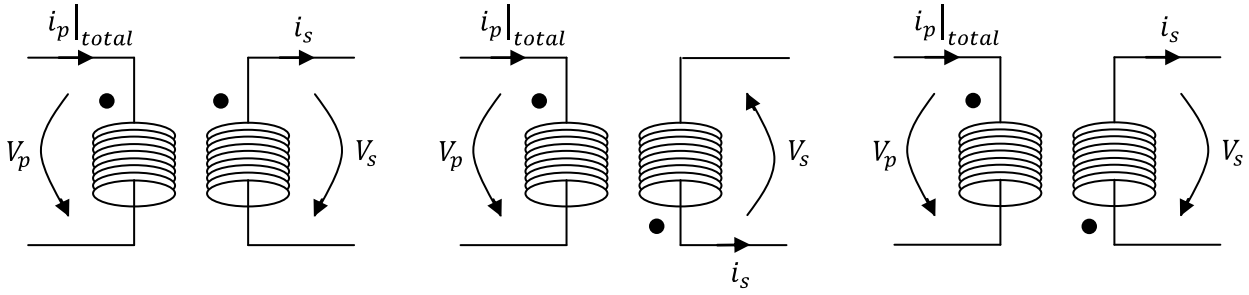



The circuit looks very similar to the circuit in the earlier paper and, indeed, it is. The only difference is the reversal of the orientation of the primary and secondary windings. Previously, in the "boost" configuration, an increasing current on the primary side developed a positive voltage at node $v_s$. In this "buck-boost" configuration, an increasing current on the primary side develops a negative voltage at node $v_s$. The dotted ends of the transformer are reversed in this schematic from their relative positions in the earlier circuit.

Let us make sure we are clear about our current conventions. In the primary circuit, the current $i_p|_{total}$ and magnetizing current $i_p$ are defined to be algebraically positive when they flow out of voltage source

$V_0$. We will define the secondary current $i_s$ to be algebraically positive when it flows in the direction in which diode $D_1$ conducts.

The voltage drop over the primary winding $v_p - v_{sw}$ will be positive when the magnetizing current in the primary circuit increases. It would be convenient to set up the circuit equations so that the voltage drop over the secondary winding $v_s$ is positive when diode $D_1$ conducts. We can do this by thinking through the following steps, starting with the "normal" transformer orientation and ending with the orientation in the circuit above.




"Normal" arrangement

$$V_s = +\frac{N_s}{N_p} V_p$$

$$i_p|_{total} = i_p + \frac{N_s}{N_p} i_s$$

Identical to "normal"

Our circuit

$$V_s = -\frac{N_s}{N_p} V_p$$

$$i_p|_{total} = i_p - \frac{N_s}{N_p} i_s$$

The "normal" orientation shown on the left is, well, normal. The step-up in voltage and current are as shown in the equations on the left-hand side. The orientation in the middle figure is identical to the normal orientation. The secondary coil has been re-drawn upside down, but the sense of the voltage and current is unchanged. The figure at the right is the same as the one in the middle, but both secondary variables, $V_s$and $i_s$, have been reversed in their direction. The equations on the right-hand side reflect the reversal the algebraic signs.

That is all there is to it. But, getting it right at the outset avoids much heartache later on.

## Part #1 – A single charging cycle

We will begin by looking at a single charging cycle. By a "charging cycle", we mean one event in which the current flowing through the primary side starts at zero (or low), and increases. The primary current must then be reduced back to zero (or low) in a following "discharging cycle" before another "charging cycle" can take place. It will take a great number of such cycles to charge the load capacitor up.

What we are doing in a charging cycle is "charging up" the energy in the magnetic field of the transformer. While the magnetic field is charging up, no current flows in the secondary circuit.

Let us assume that switch $S_1$ closes at time-base $t = 0$, before which time the circuit was at rest. For mathematical purposes, the MOSFET is modeled by its ON-resistance, $R_{on} = 0.03\Omega$. When switch $S_1$ closes, the primary circuit ceases to be an open circuit and is closed by resistor $R_{on}$. Lastly, but very importantly, we will assume that the load capacitor is charged up to some voltage $v_c|_0$ at time $t = 0$. The

load capacitor's voltage will increase slightly during each charging / discharging cycle. As we make progress charging up the load capacitor, its voltage at the start of each charging cycle will be different, and slightly higher, than it was at the start of the preceding charging cycle.

As in the earlier paper, there are six circuit variables of interest:

- $i_p\big|_{total}$ is the total current flowing through the primary circuit;
- $i_p$ is the magnetizing current flowing through the primary winding;
- $v_p - v_{sw}$ is the voltage drop over the ideal inductance in the primary winding;
- $v_s$ is the voltage drop over the ideal inductance in the secondary winding;
- $i_s$ is the total current flowing in the secondary circuit and
- $v_c$ is the voltage drop over the load capacitor.

The mathematical analysis is very simple if we recognize (and later confirm) that no current flows in the secondary circuit during the charging cycle. If that is so, then there are only two non-trivial circuit equations.

Sum of the voltage drops around the primary circuit

$$V_0 = R_{\sum p} i_p\big|_{total} + \left(v_p - v_{sw}\right) \quad (1A)$$

The magnetizing current flowing through the primary winding

Since there is no secondary current, the magnetizing current flowing through the primary winding will be the same as the total current flowing through the primary winding. Furthermore, the magnetizing current will have its traditional relationship with the voltage drop over the inductor, namely:

$$v_p - v_{sw} = L_p \frac{di_p\big|_{total}}{dt} \quad (1B)$$

These two circuit equations can be combined by inspection to give a first-order differential equation in the single variable $i_p\big|_{total}$:

$$L_p \frac{di_p\big|_{total}}{dt} + R_{\sum p} i_p\big|_{total} = V_0$$

or, using the time-constant $\tau_p = L_p / R_{\sum p}$,

$$\tau_p \frac{di_p\big|_{total}}{dt} + i_p\big|_{total} = \frac{V_0}{R_{\sum p}} \quad (2)$$

We have seen this form of equation before, and can write down the solution as:

$$i_p\big|_{total} = P e^{-\frac{t}{\tau_p}} + \frac{V_0}{R_{\sum p}}$$

The constant coefficient $P$ will be determined by the initial state of the circuit. If the circuit was completely reset during the preceding discharging cycle, then we can assume that the current flowing in the primary circuit is zero immediately before switch $S_1$ is closed. Since the magnetizing current flows through the inductor, it cannot change instantaneously, and $i_p\big|_{total}$ will still be zero immediately after switch $S_1$ is closed, and time $t$ starts ticking. Setting $i_p\big|_{total} = 0$ at time $t = 0$ in the equation above allows us to solve for $P$, and allows the waveform for $i_p\big|_{total}$ to be written as:

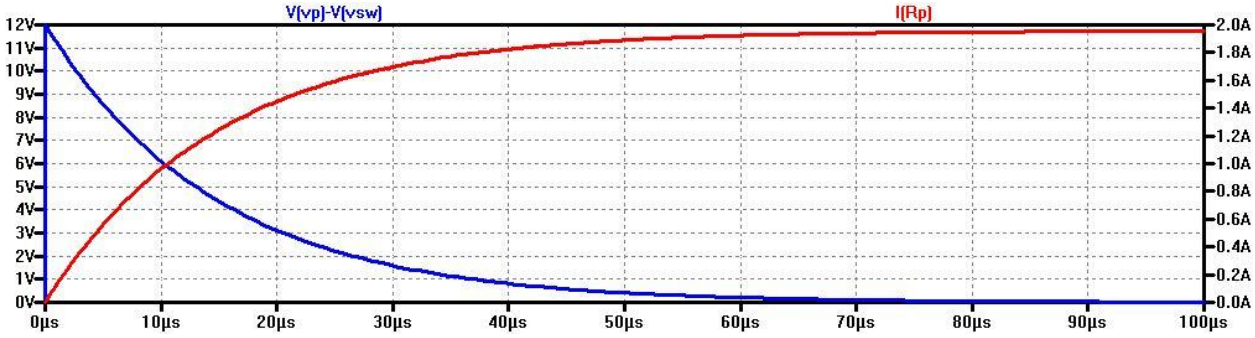
$$i_p\big|_{total} = \frac{V_0}{R_{\sum p}}\left(1 - e^{-\frac{t}{\tau_p}}\right) \quad (3)$$

Substituting $i_p\big|_{total}$ into the other circuit equation, Equation $(1B)$, gives:

$$v_p - v_{sw} = V_0 e^{-\frac{t}{\tau_p}} \quad (4)$$

It is to be noted that neither $i_p\big|_{total}$ nor $v_p - v_{sw}$ depend on the initial voltage over the capacitor. (Why not? Because no current flows through the secondary circuit during the charging cycle, it is as if the secondary circuit, and the load capacitor in it, do not exist at all.) The current $i_p\big|_{total}$ rises exponentially from zero to its steady-state value $V_0/R_{\sum p}$ with the time-constant $\tau_p$. The voltage drop over the primary winding $v_p - v_{sw}$ decreases exponentially with the time-constant $\tau_p$ from its initial value $V_0$.

The following graph from the SPICE simulation of the circuit above shows the expected waveforms for the primary current and voltage drop. (In my version of SPICE, the voltage source $V_0$ rises from zero to $12\text{V}$ during the first $20\text{ms}$ of the simulation. In order to avoid this practical but non-ideal behavior, switch $S_1$ is the circuit is not closed until $20\text{ms}$ after the simulation begins, and the results are graphed from that instant.)




It is often said that exponential changes like these are completed within five time-constants. Using our component values, five time-constants is equal to $5 \times 14.9\mu\text{s} = 74.5\mu\text{s}$.

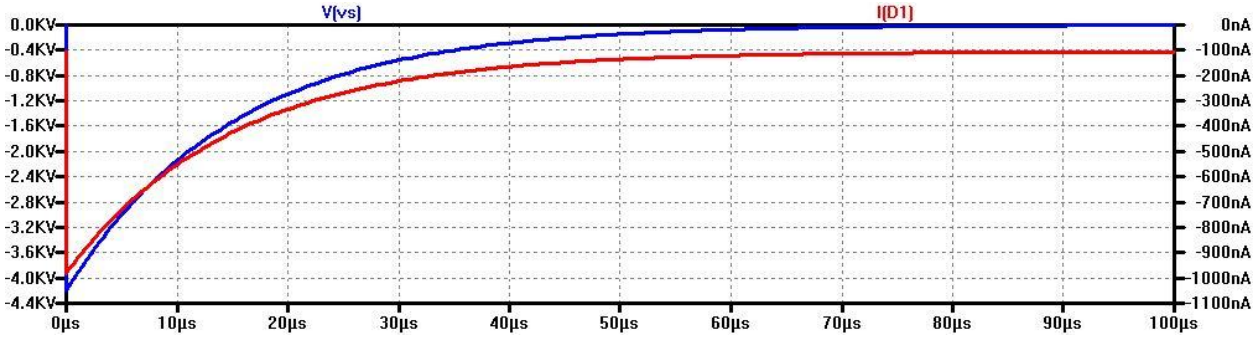
Before we leave this section, it is worthwhile to make a note of the voltage drop which exists in the secondary circuit during the charging cycle. As always, the voltage drops over the ideal primary and secondary inductances are related by the turns-ratio of the transformer, which is equal to the square root of the inductance-ratio. Therefore:

$$v_s = -\sqrt{\frac{L_s}{L_p}}\left(v_p - v_{sw}\right)$$
$$= -V_0\sqrt{\frac{L_s}{L_p}}e^{-\frac{t}{\tau_p}} \qquad (5)$$

As described above, the minus sign reflects the relative orientation of the windings. Using our component values:

$$v_s = -12\sqrt{\frac{11.2}{91.1\mu}}e^{-\frac{t}{\tau_p}}$$
$$= -4208e^{-\frac{t}{\tau_p}}\text{V}$$

The voltage drop over the secondary winding, at the start of the charging cycle, is $-4208\text{V}$. It then decays exponentially to zero. As in the earlier paper, this slightly exceeds the 4KV target voltage for the load capacitor because the secondary winding was given a few extra turns. Although there is a voltage over the secondary winding, it is in the direction which reverse-biases diode $D_1$, and no current should flow in the secondary circuit. The following graph from the SPICE simulation shows the secondary voltage drop (the SPICE variable V(vs) is shown in blue) and current (the SPICE variable I(D1) is shown in red).

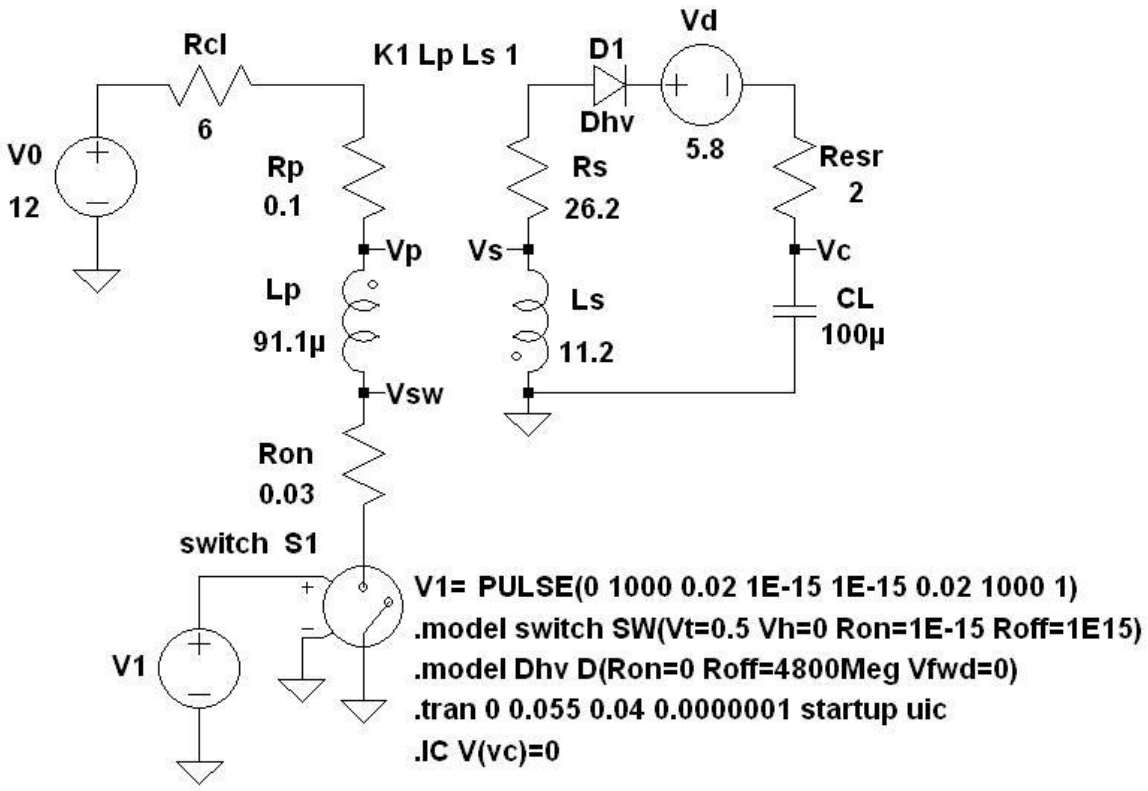



The secondary voltage drop is just as expected. However, there is a small current flowing in the secondary circuit. This is current leaking through diode $D_1$ under reverse bias. Note that the leakage current is not very large, and does not exceed about $1000\text{nA} = 1\mu\text{A}$.

## Part #2 – A single discharging cycle

In a buck-boost configuration, the interesting things do not happen when the primary circuit is "charging". They happen when the primary current is turned off. During charging, the magnetic field inside the transformer's core will build up to its steady-state value. When the primary circuit is cut off, this magnetic field will collapse. In the buck-boost configuration, there is a natural path for the escaping energy to take. It will flow into the secondary circuit, where some part of it will find its way into the load capacitor.

The circuit which we will use for the mathematical analysis and the SPICE simulation is the following.




This is the same schematic as above. The only difference is the timing of switch $S_1$. This is shown in the PULSE directive for voltage source $V_1$. Switch $S_1$ will be closed 20ms into the simulation, after the main voltage source $V_0$ has stabilized at 12V. The closing of switch $S_1$ starts the charging cycle. This time, however, switch $S_1$ opens at a time 40ms into the simulation, starting the discharge cycle which is the topic of this section. The SPICE waveforms shown out below in this Part #2 show the waveforms starting 40ms into the simulation.

Notice that the OFF-resistance of switch $S_1$, which models the OFF-resistance $R_{off}$ of the MOSFET, has been set to a very large resistance ($R_{off} = 10^{15}\Omega$). This is so much higher than the ON-resistance $R_{on}$ that I left $R_{on}$ in the circuit during the discharging cycle, simply to avoid the trouble of removing it, as I could have done.

Just to be clear about the timing, the time-base $t = 0$ for the mathematics in this Part #2 will be the instant at which the MOSFET stops conducting and its resistance changes (instantaneously) from $R_{on}$ to $R_{off}$.

In order to perform the analysis this time around, for the discharging cycle, we will need the full complement of six circuit equations.

Sum of the voltage drops around the primary circuit

$$V_0 = R_{\sum poff} i_p\big|_{total} + \left(v_p - v_{sw}\right) \quad (6A)$$

We have introduced a new symbol, $R_{\sum poff}$, for the sum of the series resistances around the primary circuit when the MOSFET stops conducting. Just so there is no uncertainty, note that:

$$\begin{aligned} R_{\sum p} &= R_{cl} + R_p + R_{on} \\ R_{\sum poff} &= R_{cl} + R_p + R_{off} \end{aligned}$$

While we are at it, let us define a corresponding time-constant as well. $\tau_p$ continues to be the time-constant based on the primary circuit's inductance and resistance during the charging cycle; $\tau_{poff}$ is the corresponding time-constant during the discharging cycle.

$$\begin{aligned} \tau_p &= L_p / R_{\sum p} \\ \tau_{poff} &= L_p / R_{\sum poff} \end{aligned}$$

Sum of the currents flowing through the primary winding

The current flowing through the primary winding will be the sum of: (i) the magnetizing current $i_p$ and (ii) the current flowing through the secondary circuit, scaled up by the turns-ratio. Because of the orientation of the two windings, this is shown algebraically with a negative sign as:

$$i_p\big|_{total} = i_p - \sqrt{\frac{L_s}{L_p}}\, i_s \quad (6B)$$

The magnetizing current of the primary winding

The magnetizing current is determined by the self-inductance of the primary winding. It is related to the voltage drop over the primary winding by:

$$v_p - v_{sw} = L_p \frac{di_p}{dt} \quad (6C)$$

The ratio of voltages between the two sides of the transformer

The voltage drops over the ideal inductances of the transformer are related by the turns-ratio, with the orientation of the two windings reflected in the minus sign, thus:

$$v_s = -\sqrt{\frac{L_s}{L_p}}\left(v_p - v_{sw}\right) \quad (6D)$$

Sum of the voltage drops around the secondary circuit

There are two cases to consider, depending on whether or not diode $D_1$ is conducting:

$$\begin{aligned} v_s = (R_s + R_{esr}) i_s + V_d + v_c \quad & (6Ea - \text{conducting}) \\ i_s = 0 \quad & (6Eb - \text{not conducting}) \end{aligned}$$

V-I characteristic of the load capacitor

The voltage drop over the load capacitor is related to the current flowing into it, and to its initial voltage, in the traditional manner. Recall that we defined $v_c|_0$ as the voltage drop over the load capacitor at the start of a charging cycle. Since no current flows in the secondary circuit during the charging cycle, the

voltage over the load capacitor remains unchanged at the end of the charging cycle, when the discharging cycle starts.

$$v_c = \frac{1}{C_L}\int_{t=0}^{t} i_s dt + v_c|_0 \quad (6F)$$

As a first step to combining these six equations, we can use Equation $(6B)$ to replace $i_p\big|_{total}$, Equation $(6C)$ to replace $v_p - v_{sw}$ and Equation $(6F)$ to replace $v_c$, in each case replacing them wherever else they occur. It is also useful to take the derivative of both Equations $(6D)$ and $(6Ea)$. We are left with three independent equations:

$$V_0 = R_{\sum poff}\left(i_p - \sqrt{\frac{L_s}{L_p}}\, i_s\right) + L_p\frac{di_p}{dt} \quad (6A')$$

$$\frac{dv_s}{dt} = -\sqrt{L_p L_s}\frac{d^2 i_p}{dt^2} \quad (6D')$$

$$\frac{dv_s}{dt} = (R_s + R_{esr})\frac{di_s}{dt} + \frac{i_s}{C_L} \quad (6Ea' - \text{conducting})$$

$$i_s = 0 \quad (6Eb' - \text{not conducting})$$

It is convenient to separate the conducting and non-conducting cases, and to pursue them separately.

## Part #2A – A single discharging cycle; conducting phase

We can re-arrange Equation $(6A')$ to isolate circuit variable $i_s$, as follows:

$$i_s = \sqrt{\frac{L_p}{L_s}}\left(\frac{L_p}{R_{\sum poff}}\frac{di_p}{dt} + i_p - \frac{V_0}{R_{\sum poff}}\right) \quad (6A'')$$

We can set equal Equation $(6Ea' - \text{conducting})$ and Equation $(6D')$, which will eliminate the derivative of $v_s$. We get:

$$-\sqrt{L_p L_s}\frac{d^2 i_p}{dt^2} = (R_s + R_{esr})\frac{di_s}{dt} + \frac{i_s}{C_L} \quad (6D'')$$

Substituting $i_s$ from Equation $(6A'')$ into Equation $(6D'')$ then gives the following second-order differential equation in the magnetizing current $i_p$.

$$-\sqrt{L_p L_s}\frac{d^2 i_p}{dt^2} = \sqrt{\frac{L_p}{L_s}}\left[(R_s + R_{esr})\frac{d}{dt}\left(\frac{L_p}{R_{\sum poff}}\frac{di_p}{dt} + i_p\right) + \frac{1}{C_L}\left(\frac{L_p}{R_{\sum poff}}\frac{di_p}{dt} + i_p - \frac{V_0}{R_{\sum poff}}\right)\right]$$

$$-L_s\frac{d^2 i_p}{dt^2} = (R_s + R_{esr})\left(\frac{L_p}{R_{\sum poff}}\frac{d^2 i_p}{dt^2} + \frac{di_p}{dt}\right) + \frac{1}{C_L}\left(\frac{L_p}{R_{\sum poff}}\frac{di_p}{dt} + i_p - \frac{V_0}{R_{\sum poff}}\right)$$

Collecting terms in the various derivatives of $i_p$ gives:

$$\left[L_s + (R_s + R_{esr})\frac{L_p}{R_{\sum poff}}\right]\frac{d^2 i_p}{dt^2} + \left[\frac{1}{C_L}\frac{L_p}{R_{\sum poff}} + (R_s + R_{esr})\right]\frac{di_p}{dt} + \frac{1}{C_L} i_p = \frac{1}{C_L}\frac{V_0}{R_{\sum poff}}$$

One further re-arrangement, in which we substitute time-constants as defined in the earlier paper, gives:

$$\left(\tau_s + \tau_{poff}\right)\frac{d^2 i_p}{dt^2} + \left(1 + \frac{\tau_{poff}}{\tau_{RC}}\right)\frac{di_p}{dt} + \frac{1}{\tau_{RC}} i_p = \frac{V_0}{\tau_{RC} R_{\sum poff}}$$

Little is to be gained by dancing around with $R_{\sum poff}$ and $\tau_{poff}$. The former is extremely large and the latter is extremely small. In the limit, as the MOSFET becomes ideal in its non-conducting mode, the differential equation reduces to:

$$\tau_s \frac{d^2 i_p}{dt^2} + \frac{di_p}{dt} + \frac{1}{\tau_{RC}} i_p = 0 \quad (7)$$

In fact, the approximation is so good that I have not troubled to use the "approximately equal to" sign.

The characteristic equation is obtained by substituting a general solution of form $i_p = e^{\gamma t}$. Since the differential equation is of the second order, the characteristic equation will be a quadratic. Its roots are:

$$\gamma_{\pm} = \frac{-1 \pm \sqrt{1 - 4\left(\frac{\tau_s}{\tau_{RC}}\right)}}{2\tau_s}$$

and the solution for $i_p$ can then be written as:

$$i_p = P_1 e^{\gamma_+ t} + P_2 e^{\gamma_- t} \quad (8)$$

The initial conditions will determine the value of the two constant coefficients $P_1$ and $P_2$. Now that we have an expression for $i_p$, we can, as before, work our way through the circuit equations to obtain expressions for the other five circuit variables. We get:

| | | |
|---|---|---|
| from Equation (8) | $i_p = P_1 e^{\gamma_+ t} + P_2 e^{\gamma_- t}$ | $(9A)$ |
| from Equation $(1C)$ | $v_p - v_{sw} = L_p(\gamma_+ P_1 e^{\gamma_+ t} + \gamma_- P_2 e^{\gamma_- t})$ | $(9B)$ |
| from Equation $(1D)$ | $v_s = -\sqrt{L_p L_s}(\gamma_+ P_1 e^{\gamma_+ t} + \gamma_- P_2 e^{\gamma_- t})$ | (9C) |
| from Equation (1A) | $i_p\big\vert_{total} = \frac{1}{R_{\sum poff}}\left[1 - L_p(\gamma_+ P_1 e^{\gamma_+ t} + \gamma_- P_2 e^{\gamma_- t})\right]$ | (9D) |

Take a look at the last equation, Equation $(9D)$, for the total primary current. $R_{\sum poff}$ is extremely large, but it is the only thing that stands between $i_p\big\vert_{total}$ and zero, so I have left it in place. Clearly, the total primary current is going to be extremely small.

The next circuit variable is $i_s$, which Equation $(1B)$ shows is proportional to $i_p - i_p\big\vert_{total}$. Since $i_p\big\vert_{total}$ is so small, one can ignore it in Equation $(1B)$, which leaves:

$$\text{from Equation (1B)} \quad i_s = \sqrt{\frac{L_p}{L_s}}\left(P_1 e^{\gamma_+ t} + P_2 e^{\gamma_- t}\right) \quad (9E)$$

The last circuit variable is the voltage $v_c$ over the load capacitor. It is determined by integration, which leads to a third unknown constant $P_3$, which will have to be found from a third initial condition:

$$\text{from Equation } (1F) \quad v_c = \sqrt{\frac{L_p}{L_s}}\frac{1}{C_L}\left[\frac{\left(1+\tau_{poff}\gamma_+\right)}{\gamma_+}P_1 e^{\gamma_+ t} + \frac{\left(1+\tau_{poff}\gamma_-\right)}{\gamma_-}P_2 e^{\gamma_- t}\right] + P_3 \quad (9F)$$

In fact, let us look now at the initial conditions. This is best done by referring back to the schematic diagram. At the end of the preceding charging cycle, just before the MOSFET is turned off, the <u>total</u> current flowing through the primary circuit will be equal to the steady-state current, $V_0/R_{\sum p}$. Since there is no current flowing in the secondary circuit, the <u>total</u> current flowing through the primary circuit is equal to the <u>magnetizing</u> current flowing through the primary inductor. The <u>magnetizing</u> current flowing through the primary inductor cannot change instantaneously. This means that, immediately after the MOSFET is turned off, the magnetizing current will still be equal to the steady-state current:

$$\begin{aligned} I.C.\#1 \qquad i_p(t=0) \quad &= \frac{V_0}{R_{\sum p}} \\ \rightarrow \qquad P_1 e^0 + P_2 e^0 \quad &= \frac{V_0}{R_{\sum p}} \\ \rightarrow \qquad P_1 + P_2 \quad &= \frac{V_0}{R_{\sum p}} \end{aligned} \quad (10A)$$

The voltage $v_c$ over the load capacitor is $v_c|_0$ immediately before the MOSFET is turned off and it, too, cannot change instantaneously. This means that:

$$\begin{aligned} I.C.\#2 \qquad v_c(t=0) \quad &= v_c|_0 \\ \rightarrow \qquad \sqrt{\frac{L_p}{L_s}}\frac{1}{C_L}\left[\frac{\left(1+\tau_{poff}\gamma_+\right)}{\gamma_+}P_1 e^0 + \frac{\left(1+\tau_{poff}\gamma_-\right)}{\gamma_-}P_2 e^0\right] + P_3 \quad &= v_c|_0 \\ \rightarrow \qquad \sqrt{\frac{L_p}{L_s}}\frac{1}{C_L}\left[\frac{\left(1+\tau_{poff}\gamma_+\right)}{\gamma_+}P_1 + \frac{\left(1+\tau_{poff}\gamma_-\right)}{\gamma_-}P_2\right] + P_3 \quad &= v_c|_0 \end{aligned} \quad (10B)$$

The third initial condition depends on the relationship between the voltage drops in the primary and secondary circuits, through the transformer, immediately after the MOSFET is turned off. Taking the sum of the voltage drops around the primary circuit at time $t = 0$, from Equation $(6A)$, gives:

$$\begin{aligned} \left(v_p - v_{sw}\right)\big|_0 \quad &= V_0 - R_{\sum poff} i_p\big|_{total}(t=0) \\ &= V_0 - R_{\sum poff}\left[\frac{V_0}{R_{\sum poff}} - \tau_{poff}\left(\gamma_+ P_1 e^0 + \gamma_- P_2 e^0\right)\right] \\ &= R_{\sum poff}\tau_{poff}\left(\gamma_+ P_1 + \gamma_- P_2\right) \\ &= L_p\left(\gamma_+ P_1 + \gamma_- P_2\right) \end{aligned}$$

Similarly, taking the sum of the voltage drops around the secondary circuit at time $t = 0$ gives:

$$\begin{aligned} v_s|_0 &= (R_s + R_{esr}) i_s(t=0) + V_d + v_c|_0 \\ &= -(R_s + R_{esr}) \sqrt{\frac{L_p}{L_s}} (P_1 e^0 + P_2 e^0) + V_d + v_c|_0 \\ &= -(R_s + R_{esr}) \sqrt{\frac{L_p}{L_s}} (P_1 + P_2) + V_d + v_c|_0 \end{aligned}$$

These voltage drops, over the ideal primary and secondary windings, are related by the turns-ratio as set out in Equation $(6D)$:

$$v_s|_0 = -\sqrt{\frac{L_s}{L_p}} \left(v_p - v_{sw}\right)\Big|_0$$

Substituting the expressions for both sides gives:

$$-(R_s + R_{esr}) \sqrt{\frac{L_p}{L_s}} (P_1 + P_2) + V_d + v_c|_0 = -\sqrt{\frac{L_s}{L_p}} L_p (\gamma_+ P_1 + \gamma_- P_2)$$

$$\rightarrow \quad \frac{1}{\tau_s}(P_1 + P_2) - \frac{V_d + v_c|_0}{\sqrt{L_p L_s}} = \gamma_+ P_1 + \gamma_- P_2$$

$$\rightarrow \quad P_1 + P_2 - \frac{\tau_s (V_d + v_c|_0)}{\sqrt{L_p L_s}} = \tau_s (\gamma_+ P_1 + \gamma_- P_2)$$

$$\rightarrow \quad (1 - \tau_s \gamma_+) P_1 + (1 - \tau_s \gamma_-) P_2 = \frac{\tau_s (V_d + v_c|_0)}{\sqrt{L_p L_s}} \qquad (10C)$$

This is the third initial condition. The three initial conditions in Equations $(10A)$ through $(10C)$ involve the three unknown constants $P_1$, $P_2$ and $P_3$. The solutions for $P_1$ and $P_2$ are:

$$P_1 = -\frac{\frac{(V_d + v_c|_0)}{\sqrt{L_p L_s}} + \left(\frac{1}{\tau_s} - \gamma_-\right) \frac{V_0}{R_{\Sigma p}}}{\gamma_+ - \gamma_-} \qquad (11A)$$

$$P_2 = \frac{\frac{(V_d + v_c|_0)}{\sqrt{L_p L_s}} + \left(\frac{1}{\tau_s} - \gamma_+\right) \frac{V_0}{R_{\Sigma p}}}{\gamma_+ - \gamma_-} \qquad (11B)$$

I have not expanded $P_3$ here, but will return to it below.

We can make some simplifying assumptions based on the relative values of the time-constants. The relative values are determined by the two principal characteristics of this type of circuit: (i) that the secondary inductance is much larger than the primary inductance and (ii) that the load capacitance is relatively large. To see the relative values, let us evaluate the time-constants using our component values. We get:

$$\tau_{poff} = \frac{L_p}{\left(R_{cl} + R_p + R_{OFF}\right)} = \frac{91.1\mu}{6 + 0.1 + 1M} = 90\text{ps} \cong 0$$
$$\tau_p = \frac{L_p}{\left(R_{cl} + R_p + R_{ON}\right)} = \frac{91.1\mu}{6 + 0.1 + 0.03} = 14.9\mu\text{s} \gg \tau_{poff}$$
$$\tau_{RC} = (R_s + R_{esr})C_L = (26.2 + 2)100\mu = 2.82\text{ms} \gg \tau_p$$
$$\tau_s = \frac{L_s}{(R_s + R_{esr})} = \frac{11.2}{26.2 + 2} = 397\text{ms} \gg \tau_{RC}$$

These inequalities are very general and will almost certainly obtain for any circuit of this type:

$$\tau_s \gg \tau_{RC} \gg \tau_p \gg \tau_{poff} \quad (12)$$

Let us begin by applying these inequalities to the angular frequencies $\gamma_+$ and $\gamma_-$.

$$\begin{aligned}\gamma_\pm &= \frac{-1 \pm \sqrt{1 - 4\left(\frac{\tau_s}{\tau_{RC}}\right)}}{2\tau_s} \\ &\cong -\frac{1}{2\tau_s} \pm j\frac{1}{\sqrt{\tau_s\tau_{RC}}} \end{aligned} \quad (13)$$

These roots have the following implication for the waveform of $i_p$, where they first arose. $i_p$ will be linear combination of two sinusoidal terms having an angular frequency of $1/\sqrt{\tau_s\tau_{RC}}$ and whose amplitudes decrease exponentially with a time-constant of $2\tau_s$.

Let us substitute these approximated forms for $\gamma_+$ and $\gamma_-$ into the expressions for $P_1$ and $P_2$. We get:

$$\begin{aligned}P_1, P_2 &= \mp\frac{\frac{(V_d + v_c|_0)}{\sqrt{L_pL_s}} + \left(\frac{1}{\tau_s} - \gamma_\mp\right)\frac{V_0}{R_{\sum p}}}{\gamma_+ - \gamma_-} \\ &\cong \mp\frac{\frac{(V_d + v_c|_0)}{\sqrt{L_pL_s}} + \left(\frac{1}{\tau_s} + \frac{1}{2\tau_s} \mp j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right)\frac{V_0}{R_{\sum p}}}{j\frac{2}{\sqrt{\tau_s\tau_{RC}}}} \\ &= \pm\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \left(\frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}} \mp j\right)\frac{V_0}{R_{\sum p}}\right] \\ &= \pm\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}}\frac{V_0}{R_{\sum p}}\right] + \frac{1}{2}\frac{V_0}{R_{\sum p}} \end{aligned} \quad (14)$$

It will be useful to have in our back pocket the following expressions involving the $\gamma$'s:

$$\gamma_+ + \gamma_- = \left(-\frac{1}{2\tau_s} + j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right) + \left(-\frac{1}{2\tau_s} - j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right) = -\frac{1}{\tau_s} \tag{15A}$$

$$\gamma_+ - \gamma_- = \left(-\frac{1}{2\tau_s} + j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right) - \left(-\frac{1}{2\tau_s} - j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right) = j\frac{2}{\sqrt{\tau_s\tau_{RC}}} \tag{15B}$$

$$\begin{aligned}\gamma_+^2 + \gamma_-^2 &= \left(-\frac{1}{2\tau_s} + j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right)^2 + \left(-\frac{1}{2\tau_s} - j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right)^2 \\ &= \left(\frac{1}{4\tau_s^2} - \frac{j}{\tau_s\sqrt{\tau_s\tau_{RC}}} - \frac{1}{\tau_s\tau_{RC}}\right) + \left(\frac{1}{4\tau_s^2} + \frac{j}{\tau_s\sqrt{\tau_s\tau_{RC}}} - \frac{1}{\tau_s\tau_{RC}}\right) \\ &= -\frac{2}{\tau_s\tau_{RC}}\left(1 - \frac{\tau_{RC}}{4\tau_s}\right)\end{aligned} \tag{15C}$$

$$\begin{aligned}\gamma_+^2 - \gamma_-^2 &= \left(-\frac{1}{2\tau_s} + j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right)^2 - \left(-\frac{1}{2\tau_s} - j\frac{1}{\sqrt{\tau_s\tau_{RC}}}\right)^2 \\ &= \left(\frac{1}{4\tau_s^2} - \frac{j}{\tau_s\sqrt{\tau_s\tau_{RC}}} - \frac{1}{\tau_s\tau_{RC}}\right) - \left(\frac{1}{4\tau_s^2} + \frac{j}{\tau_s\sqrt{\tau_s\tau_{RC}}} - \frac{1}{\tau_s\tau_{RC}}\right) \\ &= -j\frac{2}{\tau_s\sqrt{\tau_s\tau_{RC}}}\end{aligned} \tag{15D}$$

and the following expressions involving the $\gamma$'s and the $P$'s:

$$\begin{aligned}\gamma_+P_1 + \gamma_-P_2 &= (\gamma_+ - \gamma_-)\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}}\frac{V_0}{R_{\sum p}}\right] + (\gamma_+ + \gamma_-)\frac{1}{2}\frac{V_0}{R_{\sum p}} \\ &= \left(j\frac{2}{\sqrt{\tau_s\tau_{RC}}}\right)\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}}\frac{V_0}{R_{\sum p}}\right] - \frac{1}{\tau_s}\frac{1}{2}\frac{V_0}{R_{\sum p}} \\ &= -\frac{V_d + v_c|_0}{\sqrt{L_pL_s}} - \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\end{aligned} \tag{16A}$$

$$\begin{aligned}\gamma_+^2P_1 + \gamma_-^2P_2 &= (\gamma_+^2 - \gamma_-^2)\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}}\frac{V_0}{R_{\sum p}}\right] + (\gamma_+^2 + \gamma_-^2)\frac{1}{2}\frac{V_0}{R_{\sum p}} \\ &= \left(-j\frac{2}{\tau_s\sqrt{\tau_s\tau_{RC}}}\right)\frac{j}{2}\left[\sqrt{\frac{C_L}{L_p}}(V_d + v_c|_0) + \frac{3}{2}\sqrt{\frac{\tau_{RC}}{\tau_s}}\frac{V_0}{R_{\sum p}}\right] - \frac{2}{\tau_s\tau_{RC}}\left(1 - \frac{\tau_{RC}}{4\tau_s}\right)\frac{1}{2}\frac{V_0}{R_{\sum p}} \\ &= \frac{1}{\tau_s}\left[\frac{V_d + v_c|_0}{\sqrt{L_pL_s}} - \frac{1}{\tau_{RC}}\left(1 - \frac{7\tau_{RC}}{4\tau_s}\right)\frac{V_0}{R_{\sum p}}\right]\end{aligned} \tag{16B}$$

And, we can also make a simplifying assumption regarding time. $i_p$, for example, is a waveform which decays exponentially with time. But, the discharging cycle occupies only a small part of the complete decay process. We can approximate the exponential function, which is a curve, by a linear function of time, which is a straight line, for the small part in which we are interested. If $\gamma_+t$ and $\gamma_-t$ are small, then we can use the Taylor series expansion and approximation for the exponential function, that $e^x \cong 1 + x$ for small $x$. Then, we can approximate as follows:

$$e^{\gamma_+ t} \cong 1 + \gamma_+ t \quad (17A)$$
$$e^{\gamma_- t} \cong 1 + \gamma_- t \quad (17B)$$

With the two sets of simplifying assumptions, we can go back to Equations (9) and expand the expressions for the circuit variables.

For $i_s$, we get:

$$\begin{aligned} i_s &= \sqrt{\frac{L_p}{L_s}}(P_1 e^{\gamma_+ t} + P_2 e^{\gamma_- t}) \\ &\cong \sqrt{\frac{L_p}{L_s}}[(1+\gamma_+ t)P_1 + (1+\gamma_- t)P_2] \\ &= \sqrt{\frac{L_p}{L_s}}[(P_1+P_2) + (\gamma_+ P_1 + \gamma_- P_2)t] \\ &\cong \sqrt{\frac{L_p}{L_s}}\left[\frac{V_0}{R_{\sum p}} - \left(\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} + \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\right)t\right] \end{aligned} \quad (18A)$$

For $v_s$, we get:

$$\begin{aligned} v_s &= -\sqrt{L_p L_s}(\gamma_+ P_1 e^{\gamma_+ t} + \gamma_- P_2 e^{\gamma_- t}) \\ &\cong -\sqrt{L_p L_s}[(1+\gamma_+ t)\gamma_+ P_1 + (1+\gamma_- t)\gamma_- P_2] \\ &= -\sqrt{L_p L_s}[(\gamma_+ P_1 + \gamma_- P_2) + (\gamma_+^2 P_1 + \gamma_-^2 P_2)t] \\ &\cong -\sqrt{L_p L_s}\left[\left(-\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\right) + \frac{1}{\tau_s}\left[\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{1}{\tau_{RC}}\left(1 - \frac{7\tau_{RC}}{4\tau_s}\right)\frac{V_0}{R_{\sum p}}\right]t\right] \\ &= \left(V_d + v_c|_0 + \frac{2\sqrt{L_p L_s}}{\tau_s}\frac{V_0}{R_{\sum p}}\right) - \frac{1}{\tau_s}\left[V_d + v_c|_0 - \frac{\sqrt{L_p L_s}}{\tau_{RC}}\left(1 - \frac{\cancel{7\tau_{RC}}}{\cancel{4\tau_s}}\right)\frac{V_0}{R_{\sum p}}\right]t \\ &\cong \left(V_d + v_c|_0 + \frac{2\sqrt{L_p L_s}}{\tau_s}\frac{V_0}{R_{\sum p}}\right) - \frac{1}{\tau_s}\left(V_d + v_c|_0 - \frac{\sqrt{L_p L_s}}{\tau_{RC}}\frac{V_0}{R_{\sum p}}\right)t \end{aligned} \quad (18B)$$

And, for $v_p - v_{sw}$, we get:

$$\begin{aligned} v_p - v_{sw} &= L_p(\gamma_+ P_1 e^{\gamma_+ t} + \gamma_- P_2 e^{\gamma_- t}) \\ &\cong L_p[\gamma_+ P_1(1+\gamma_+ t) + \gamma_- P_2(1+\gamma_- t)] \\ &= L_p(\gamma_+ P_1 + \gamma_- P_2) + L_p(\gamma_+^2 P_1 + \gamma_-^2 P_2)t \\ &\cong L_p\left(-\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\right) + L_p\left\{\frac{1}{\tau_s}\left[\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{1}{\tau_{RC}}\left(1 - \frac{7\tau_{RC}}{4\tau_s}\right)\frac{V_0}{R_{\sum p}}\right]\right\}t \\ &= -\left[\sqrt{\frac{L_p}{L_s}}(V_d + v_c|_0) + \frac{2L_p}{\tau_s}\frac{V_0}{R_{\sum p}}\right] + \frac{L_p}{\tau_s}\left[\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{1}{\tau_{RC}}\left(1 - \frac{\cancel{7\tau_{RC}}}{\cancel{4\tau_s}}\right)\frac{V_0}{R_{\sum p}}\right]t \end{aligned}$$

And, lastly:

$$v_p - v_{sw} \quad \cong -\left[\sqrt{\frac{L_p}{L_s}}(V_d + v_c|_0) + \frac{2L_p}{\tau_s}\frac{V_0}{R_{\sum p}}\right] + \frac{L_p}{\tau_s}\left(\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} - \frac{1}{\tau_{RC}}\frac{V_0}{R_{\sum p}}\right)t \quad (18C)$$

All of these expressions have linear dependence on time. The one of immediate interest is the secondary current $i_s$. Equation $(18A)$ shows that it is initially positive and that it decreases linearly with time thereafter. This has two consequences: (i) that $i_s$ is initially positive, which means that current flows through diode $D_1$ in the positive direction, in its conduction mode, and (ii) that, at some time after the discharging cycle begins, the secondary current will fall to zero.

We can calculate the time $t = T_{stop}$ at which the secondary current reaches zero and at which diode $D_1$ stops conducting. This will happen when the expression in Equation $(18A)$, for $i_s$, reaches zero.

$$\frac{V_0}{R_{\sum p}} - \left(\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} + \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\right)T_{stop} = 0$$

$$\rightarrow \quad T_{stop} = \frac{\frac{V_0}{R_{\sum p}}}{\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} + \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}}$$

$$\rightarrow \quad T_{stop} = \frac{\tau_s}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c|_0}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 2} \quad (19)$$

How does the duration of the conduction period vary with the initial voltage on the capacitor? Using our component values, Equation (19) becomes:

$$T_{stop} \quad = \frac{0.397}{\sqrt{\frac{11.2}{91.1\mu}\left(\frac{5.8 + v_c|_0}{12}\right)\left(\frac{6.13}{26.2 + 2}\right)} + 2}$$

$$= \frac{0.397}{38.84 + 6.352 v_c|_0} \quad (19')$$

$T_{stop}$ will be a positive time for all initial capacitor voltages. In other words, the charging procedure will never stop. This has huge implications for this application. It means that the voltage that we can place on the capacitor is not limited to the supply voltage $V_0$ as stepped up by the turns-ratio. In practice, though, I expect that the response time of the components, which we have ignored, will eventually become important compared with the theoretical stop time. We will have to look more carefully at this matter below.

When the initial capacitor voltage is zero, the stop time is $T_{stop} = 0.397/38.84 = 10.22\text{ms}$. At an initial capacitor voltage of $500\text{V}$, the stop time is $T_{stop} = 0.397/3215 = 123.5\mu\text{s}$. By the time the load capacitor reaches a voltage of $3000\text{V}$, the stop time will have decreased to $T_{stop} = 0.397/19{,}090 = 20.79\mu\text{s}$. The stop time will reach $2\mu s$ when the capacitor's voltage reaches $v_c|_0 = 31{,}240\text{V}$. This is well about the target voltage we are aiming for, but does illustrate one thing. The period $2\mu s$ corresponds to a frequency of $500\text{KHz}$, which is at the bottom of the A.M. radio band. At this point, electrons will be racing up and down the wires in the secondary circuit fast enough for energy to begin to be radiated away.

This is an example of the kinds of effects which will prevent the load capacitor from charging without limit.

Nor should we lose sight of the fact that the ferrite core of our transformer works best at cycling periods in the range from $2.5\mu s$ to $100\mu s$. I am not sure about all of the implications of cycling more quickly or more slowly than this, but it will certainly mean that the transfer of energy from the primary side to the secondary side will not be as complete as predicted. Some energy will be lost in the core, and not find its way into the load capacitor.

It is well to ask: what capacitor voltage corresponds to a minimum cycling period for our ferrite core? Setting $T_{stop} = 2.5\mu s$ in Equation $(19')$ gives $v_c|_0 = 24{,}990\text{V}$.

Before running the SPICE simulation, let us evaluate the expressions for some of the circuit variables, using our component values, but leaving unspecified the initial capacitor voltage $v_c|_0$.

For $i_s$, Equation $(18A)$ becomes:

$$\begin{aligned} i_s &\cong \sqrt{\frac{91.1\mu}{11.2}}\left[\frac{12}{6.13} - \left(\frac{5.8 + v_c|_0}{\sqrt{91.1\mu \times 11.2}} + \frac{2}{0.397}\frac{12}{6.13}\right)t\right] \\ &= 0.005583 - (0.5460 + 0.08929 v_c|_0)t \end{aligned}$$

For $v_s$, Equation $(18B)$ becomes:

$$\begin{aligned} v_s &\cong \left\{ \begin{array}{l} \left(5.8 + v_c|_0 + \dfrac{2\sqrt{91.1\mu \times 11.2}}{0.397}\dfrac{12}{6.13}\right) + \\ -\dfrac{1}{0.397}\left(5.8 + v_c|_0 - \dfrac{\sqrt{91.1\mu \times 11.2}}{0.00282}\dfrac{12}{6.13}\right)t \end{array} \right\} \\ &= (6.115 + v_c|_0) + (41.24 - 2.519 v_c|_0)t \end{aligned}$$

For $v_p - v_{sw}$, Equation $(18C)$ becomes:

$$\begin{aligned} v_p - v_{sw} &\cong \left\{ \begin{array}{l} -\left[\sqrt{\dfrac{91.1\mu}{11.2}}(5.8 + v_c|_0) + \dfrac{2 \times 91.1\mu}{0.397}\dfrac{12}{6.13}\right] + \cdots \\ \cdots + \dfrac{91.1\mu}{0.397}\left(\dfrac{5.8 + v_c|_0}{\sqrt{91.1\mu \times 11.2}} - \dfrac{1}{0.00282}\dfrac{12}{6.13}\right)t \end{array} \right\} \\ &= -(0.01744 + 0.002852 v_c|_0) + (-0.1176 + 0.007184 v_c|_0)t \end{aligned}$$

For $i_p\big|_{total}$, Equation $(6A)$ becomes:

$$\begin{aligned} i_p\big|_{total} &= \frac{1}{R_{\sum poff}}\left[V_0 - (v_p - v_{sw})\right] \\ &\cong \frac{1}{R_{\sum poff}}[12 + (0.01744 + 0.002852 v_c|_0) - (-694.1 + 0.007184 v_c|_0)t] \\ &= 10^{-6} \times [(12.02 + 0.002852 v_c|_0) + (694.1 - 0.007184 v_c|_0)t] \end{aligned}$$

Now, for each of these four circuit variables, let us calculate the expressions for three different initial voltages over the load capacitor.

| $v_c\|_0 \rightarrow$ | 0V | 500V | 3000V |
|---|---|---|---|
| $i_s =$ | $(5.583 - 546.0t)$mA | $(5.583 - 45{,}190t)$mA | $(5.583 - 268{,}400t)$mA |
| $v_s =$ | $(6.115 + 41.24t)$V | $(506.1 - 1218t)$V | $(3006 - 7516t)$V |
| $v_p - v_{sw} =$ | $-(0.01744 + 0.1176t)$V | $-(1.443 - 3.474t)$V | $-(8.573 - 21.43t)$V |
| $i_p\|_{total} =$ | $(12.02 + 694.1t)$µA | $(13.45 + 693.2t)$µA | $(20.58 + 672.5t)$µA |

Let us take one final step. We will evaluate the four circuit variables at two times, $t = 0$ and $t = T_{stop}$.

| $v_c\|_0 \rightarrow$ | 0V | 0V | 500V | 500V | 3000V | 3000V |
|---|---|---|---|---|---|---|
| $t =$ | 0 | $T_{stop} = 10.22$ms | 0 | $T_{stop} = 123.5$µs | 0 | $T_{stop} = 20.79$µs |
| $i_s =$ | 5.583mA | 0 | 5.583mA | 0 | 5.583mA | 0 |
| $v_s =$ | 6.115V | 6.536V | 506.1V | 505.9V | 3006V | 3005.8V |
| $v_p - v_{sw} =$ | −17.44mV | −18.64mV | −1.443V | −1.443V | −8.573V | −8.573V |
| $i_p\|_{total}$ | 12.02µA | 19.11µA | 13.45µA | 13.54µA | 20.58µA | 20.59µA |

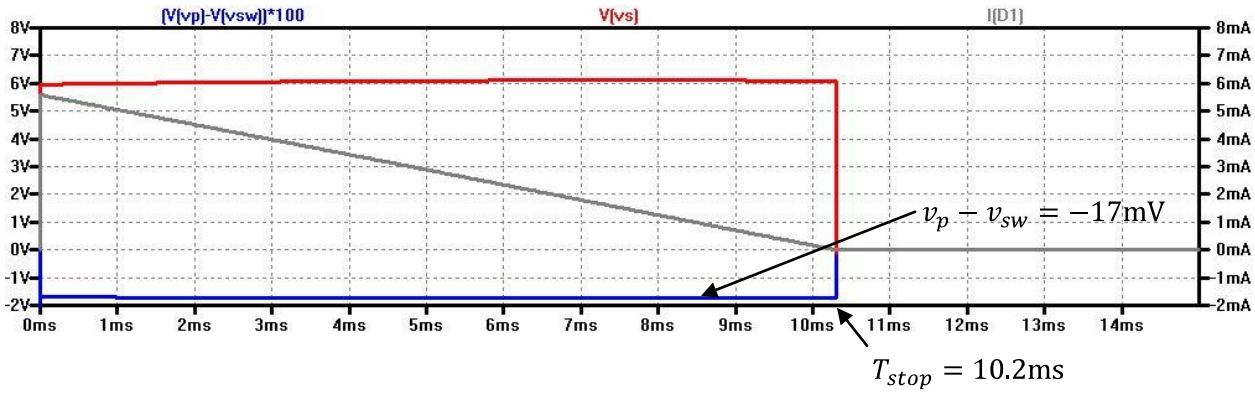
Observations:

- the secondary current starts out at the primary circuit's steady-state current, stepped down by the turns-ratio, and decreases linearly to zero in time $T_{stop}$;
- for all intents and purposes, the secondary voltage remains constant throughout the discharging cycle at a voltage equal to diode $D_1$'s forward voltage drop plus the initial voltage over the load capacitor;
- except for very low initial capacitor voltages, the voltage drop over the ideal primary inductance also remains constant throughout the charging cycle and
- the total primary current $i_p\|_{total}$ is extremely small.

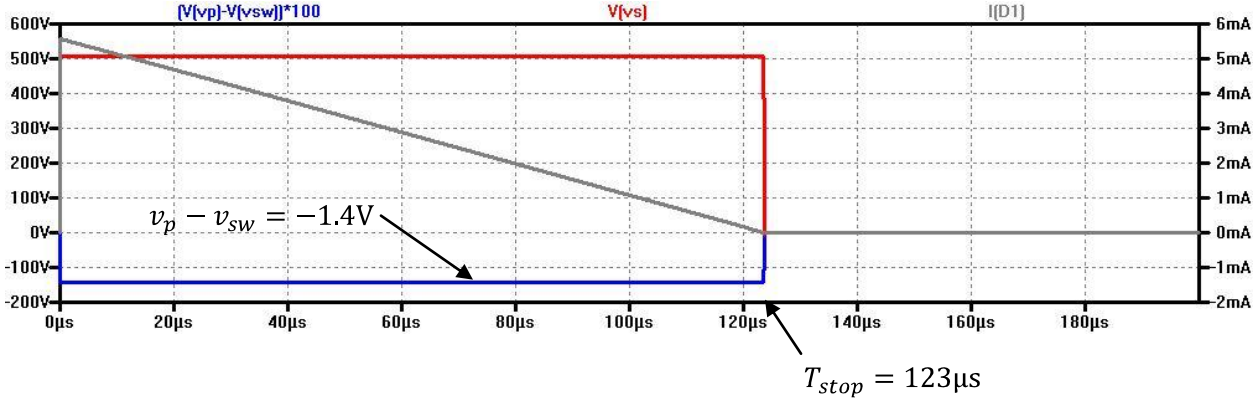
To examine the accuracy of the circuit equations and the appropriateness of the approximations made, the SPICE model was run three times, once for each of the three initial voltages over the capacitor: 0V, 500V and 3000V. The following graphs show the results obtained. In each graph, the following three circuit variables are shown:

- the voltage drop $v_p - v_{sw}$ over the ideal primary inductance is plotted in blue. The corresponding SPICE parameter names are V(vp)-V(vsw). Note that $v_p - v_{sw}$ is multiplied by a scaling factor of 100 so that it is comparable in size to $v_s$ in the display;
- the voltage drop $v_s$ over the ideal secondary inductance is plotted in red. The corresponding SPICE parameter name is V(vs) and
- the current $i_s$ flowing in the secondary circuit is plotted in gray. The current through diode $D_1$, which is the SPICE parameter I(D1), is used as the proxy for $i_s$.

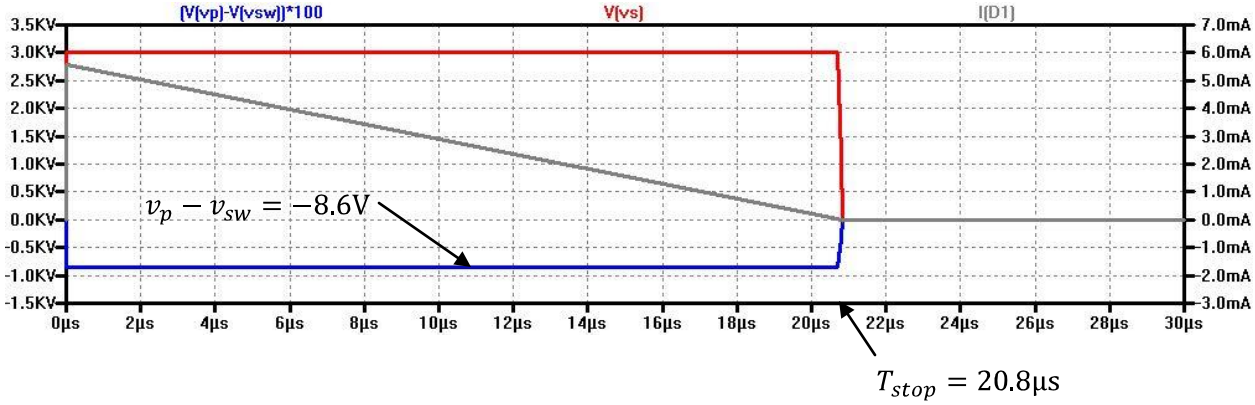
For the uncharged capacitor, the waveforms are as follows:




When the load capacitor is initially charged to 500V, the waveforms are:




When the load capacitor is initially charged to 3000V, the waveforms are:




Our mathematical analysis agrees remarkably well with the SPICE simulation.

## Part 3 – The efficiency with which energy is transferred

During the charging cycle, the current flowing through the primary circuit builds up to its steady state value in accordance with Equation (3):

$$i_p\big|_{total} = \frac{V_0}{R_{\Sigma p}}\left(1 - e^{-\frac{t}{\tau_p}}\right) \quad (3)$$

The power supplied by the power supply at any instant during charging is equal to $V_0 \times i_p\big|_{total}$. We can find the cumulative energy supplied by the power supply $E_{PS}$ by integrating the instantaneous power from time $t = 0$ until some given time $t = T$, thus:

$$\begin{aligned} E_{PS}(t=T) &= \frac{V_0^2}{R_{\sum p}} \int_{t=0}^{t=T} \left(1 - e^{-\frac{t}{\tau_p}}\right) dt \\ &= \frac{V_0^2}{R_{\sum p}} \left(t + \tau_p e^{-\frac{t}{\tau_p}}\right)\Big|_{t=0}^{t=T} \\ &= \frac{V_0^2}{R_{\sum p}} \left[(T-0) + \left(\tau_p e^{-\frac{T}{\tau_p}} - \tau_p e^{0}\right)\right] \\ &= \frac{V_0^2}{R_{\sum p}} \left[T + \tau_p \left(e^{-\frac{T}{\tau_p}} - 1\right)\right] \end{aligned} \quad (20)$$

At any given time, the energy stored in the magnetic field $E_{MF}$ by the current flowing through the primary winding is given by the traditional formula:

$$E_{MF} = \frac{1}{2} L_p i_p^2 \quad (21)$$

As the steady-state is approached, the energy stored in the magnetic field approaches a constant, maximum value. However, the cumulative energy supplied by the power supply continues to increase, as power is burned off by the resistors in the primary circuit. It is important that we bring the charging cycle to an end once the primary current gets "close enough" to its steady-state value. Otherwise, we will be wasting energy. Let us choose, a little bit arbitrarily, to end the charging cycle after five $\tau_p$ time-constants. By then, the cumulative energy delivered by the power supply will be equal to:

$$\begin{aligned} E_{PS}(t=5\tau_p) &= \frac{V_0^2}{R_{\sum p}} \left[5\tau_p + \tau_p \left(e^{-\frac{5\tau_p}{\tau_p}} - 1\right)\right] \\ &\cong \frac{V_0^2}{R_{\sum p}} \left(5\tau_p - \tau_p\right) \\ &= 4\tau_p \frac{V_0^2}{R_{\sum p}} \end{aligned} \quad (22)$$

and the energy stored in the magnetic field will be very close to its steady-state value:

$$\begin{aligned} E_{MF}(t=5\tau_p) &\cong \frac{1}{2} L_p i_{pSS}^2 \\ &= \frac{1}{2} L_p \left(\frac{V_0}{R_{\sum p}}\right)^2 \end{aligned} \quad (23)$$

At that particular point in time, the fraction of the energy supplied which has found its way into the magnetic field is equal to:

$$\frac{E_{MF}(t=5\tau_p)}{E_{PS}(t=5\tau_p)} \cong \frac{1}{2}L_p\left(\frac{V_0}{R_{\sum p}}\right)^2\frac{1}{4\tau_p}\frac{R_{\sum p}}{V_0^2} = \frac{1}{8} \qquad (24)$$

So, during the charging cycle, only one-eighth of the energy supplied by the power supply is stored in the magnetic field. The other seven-eighths have been converted into heat as the current was forced to flow through the resistors in the primary circuit. The biggest contributor to those resistances and losses is $R_{cl}$ – the current limiting resistor – which we added to the circuit purposefully to limit the current to the 2A acceptable to the power supply. Removing or reducing $R_{cl}$ would allow things to be speeded up, and would reduce the absolute amount of energy wasted, but would not change the efficiency. The 12.5% efficiency of the charging cycle is a fundamental consequence of waiting five time-constants. But, if it becomes necessary to speed things up, reducing the length of the charging cycle to four time-constants, or perhaps even three, would be worth considering.

Now, let us move on and consider the discharging cycle. During the discharging cycle, energy from the magnetic field is converted into current flowing in the secondary circuit, some part of which finds its way onto the capacitor. We have already determined that the secondary current flowing during the discharge cycle is given by:

$$i_s = \sqrt{\frac{L_p}{L_s}}\left[\frac{V_0}{R_{\sum p}} - \left(\frac{V_d + v_c|_0}{\sqrt{L_p L_s}} + \frac{2}{\tau_s}\frac{V_0}{R_{\sum p}}\right)t\right] \qquad (18A)$$

The three important characteristics of this waveform are:

- the secondary current starts with a value of $\sqrt{\frac{L_p}{L_s}}\frac{V_0}{R_{\sum p}}$;
- it decreases linearly with time thereafter until
- it stops at time $t = T_{stop} = \frac{\tau_s}{\sqrt{\frac{L_s}{L_p}}\left(\frac{V_d+v_c|_0}{V_0}\right)\left(\frac{R_{\sum p}}{R_s+R_{esr}}\right)+2}$.

Geometrically, the waveform is the hypotenuse of a right triangle. The average current which flows during the discharging cycle is therefore equal to one-half of the height (that is, the starting current) of the right triangle, thus:

$$i_s|_{avg} = \frac{1}{2}\sqrt{\frac{L_p}{L_s}}\frac{V_0}{R_{\sum p}} \qquad (25)$$

The average current multiplied by $T_{stop}$ is therefore equal to the charge $\Delta Q$ which is transported during the discharging cycle, and which is added to the charge already present in the load capacitor. Therefore:

$$\Delta Q = \frac{1}{2}\sqrt{\frac{L_p}{L_s}}\frac{V_0}{R_{\sum p}}\left[\frac{\tau_s}{\sqrt{\frac{L_s}{L_p}}\left(\frac{V_d + v_c|_0}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right) + 2}\right]$$

and, continuing:

$$\begin{aligned}\Delta Q &= \frac{\frac{1}{R_s + R_{esr}} \frac{\sqrt{L_p L_s}}{2} \frac{V_0}{R_{\sum p}}}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c|_0}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + \cancel{2}} \\ &\cong \frac{1}{2}\left(\frac{L_p}{V_d + v_c|_0}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2 \qquad (26)\end{aligned}$$

Now, the charge stored in the load capacitor and the voltage drop over it are related by the traditional formula:

$$Q = C_L v_c \quad (27)$$

If we let $Q_0$ be the charge on the capacitor when its voltage is $v_c = v_c|_0$, then the addition of charge $\Delta Q$ will raise the capacitor's voltage by $\Delta v_c$, and $\Delta Q$ and $\Delta v_c$ will be related by:

$$\begin{aligned} & Q_0 + \Delta Q = C_L(v_c|_0 + \Delta v_c) \\ \rightarrow \quad & Q_0 + \Delta Q = C_L v_c|_0 + C_L \Delta v_c \\ \rightarrow \quad & \Delta Q = C_L \Delta v_c \qquad (28)\end{aligned}$$

Substituting Equation (26) into Equation (28) gives:

$$\Delta v_c = \frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c|_0}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2 \quad (29)$$

From a standing start, the change in voltage over the load capacitor during the first, second and third discharging cycles, respectively, are:

$$\begin{aligned}\Delta v_c|_{cycle\ \#1} &= \frac{91.1\mu}{2 \times 100\mu}\left(\frac{1}{5.8 + 0}\right)\left(\frac{12}{6.13}\right)^2 = 0.301\text{V} \\ \Delta v_c|_{cycle\ \#2} &= \frac{91.1\mu}{2 \times 100\mu}\left(\frac{1}{5.8 + 0.301}\right)\left(\frac{12}{6.13}\right)^2 = 0.286\text{V} \\ \Delta v_c|_{cycle\ \#3} &= \frac{91.1\mu}{2 \times 100\mu}\left(\frac{1}{5.8 + 0.587}\right)\left(\frac{12}{6.13}\right)^2 = 0.273\text{V}\end{aligned}$$

By the time the load capacitor's voltage has reached $500\text{V}$, the increase in voltage during one discharging cycle will have decreased to:

$$\Delta v_c|_{500\text{V}} = \frac{91.1\mu}{2 \times 100\mu}\left(\frac{1}{5.8 + 500}\right)\left(\frac{12}{6.13}\right)^2 = 0.00345\text{V}$$

Now, let us look at the energy stored in the capacitor. The energy and voltage of the load capacitor at any instant in time are related by the traditional formula:

$$E_{C_L} = \frac{1}{2} C_L v_c^2 \quad (30)$$

Suppose we define $\Delta E_{C_L}$ as the change in energy during one discharging cycle. We will use whatever subscript is necessary to identify the discharging cycle. Letting $v_c|_0$ be the voltage at the start of the discharging cycle and $\Delta v_c$ be the change in voltage during the cycle, we can write:

$$\begin{aligned} \Delta E_{C_L} &= \frac{1}{2} C_L (v_c|_0 + \Delta v_c)^2 - \frac{1}{2} C_L (v_c|_0)^2 \\ &= \frac{1}{2} C_L [2 v_c|_0 \Delta v_c + (\Delta v_c)^2] \\ &= \frac{1}{2} C_L \Delta v_c (2 v_c|_0 + \Delta v_c) \end{aligned}$$

I hesitate to approximate away the term $\Delta v_c$ in the round brackets because it is the only applicable term when the capacitor's initial voltage is small. Substituting Equation (29) gives:

$$\Delta E_{C_L} = \frac{L_p}{4} \left( \frac{1}{V_d + v_c|_0} \right) \left( \frac{V_0}{R_{\sum p}} \right)^2 \left[ 2 v_c|_0 + \frac{L_p}{2 C_L} \left( \frac{1}{V_d + v_c|_0} \right) \left( \frac{V_0}{R_{\sum p}} \right)^2 \right] \quad (31)$$

The increase in the energy stored in the load capacitor during the first, second and third discharging cycles, respectively, are:

$$\begin{aligned} \Delta E_{C_L}\big|_{cycle\ \#1} &= \frac{91.1\mu}{4} \left( \frac{1}{5.8 + 0} \right) \left( \frac{12}{6.13} \right)^2 \left[ 0 + \frac{91.1\mu}{200\mu} \left( \frac{1}{5.8} \right) \left( \frac{12}{6.13} \right)^2 \right] = 4.53\mu J \\ \Delta E_{C_L}\big|_{cycle\ \#2} &= \frac{91.1\mu}{4} \left( \frac{1}{5.8 + 0.301} \right) \left( \frac{12}{6.13} \right)^2 \left[ 0.602 + \frac{91.1\mu}{200\mu} \left( \frac{1}{6.101} \right) \left( \frac{12}{6.13} \right)^2 \right] = 12.7\mu J \\ \Delta E_{C_L}\big|_{cycle\ \#3} &= \frac{91.1\mu}{4} \left( \frac{1}{5.8 + 0.587} \right) \left( \frac{12}{6.13} \right)^2 \left[ 1.174 + \frac{91.1\mu}{200\mu} \left( \frac{1}{6.387} \right) \left( \frac{12}{6.13} \right)^2 \right] = 19.8\mu J \end{aligned}$$

By the time the load capacitor's voltage has reached $500V$, the increase in energy during one discharging cycle will have increased to:

$$\Delta E_{C_L}\big|_{500V} = \frac{91.1\mu}{4} \left( \frac{1}{5.8 + 500} \right) \left( \frac{12}{6.13} \right)^2 \left[ 1000 + \frac{91.1\mu}{200\mu} \left( \frac{1}{505.8} \right) \left( \frac{12}{6.13} \right)^2 \right] = 173\mu J$$

Comparing these values for $\Delta E_{C_L}$ with the values above for $\Delta v_c$ show that, as the charging procedure advances, the successive increments to the load capacitor's voltage decrease but the successive increments to the load capacitor's energy increase. This has huge implications for the application. As time passes during the charging procedure, the rate at which energy is stored in the capacitor actually increases.

In each of these discharging cycles, the energy which had been built up in the magnetic field during the preceding charging cycle [given in Equation (23) above] is equal to (a constant):

$$E_{MF}(t = 5\tau_p) = \frac{91.1\mu}{2} \left( \frac{12}{6.13} \right)^2 = 175\mu J$$

So, the efficiency with which energy is transferred from the magnetic field to the capacitor during the first three discharging cycles are as follows:

$$\frac{\Delta E_{C_L}\big|_{cycle\ \#1}}{E_{MF}(t = 5\tau_p)} = \frac{4.53\mu J}{175\mu J} = 2.6\%$$
$$\frac{\Delta E_{C_L}\big|_{cycle\ \#2}}{E_{MF}(t = 5\tau_p)} = \frac{12.7\mu J}{175\mu J} = 7.3\%$$
$$\frac{\Delta E_{C_L}\big|_{cycle\ \#3}}{E_{MF}(t = 5\tau_p)} = \frac{19.8\mu J}{175\mu J} = 11.3\%$$

The efficiency with which energy is transferred from the magnetic field to the load capacitor when it has reached $500V$ is:

$$\frac{\Delta E_{C_L}\big|_{500V}}{E_{MF}(t = 5\tau_p)} = \frac{173\mu J}{175\mu J} = 99\%$$

Observations:

- The efficiency of the discharging cycle is almost $100\%$. During the discharging cycle, virtually all of the energy stored in the magnetic field is transferred into the capacitor.
- The efficiency of the charging cycle is determined by the number of time-constants we, as the designers, are prepared to wait. At five time-constants, one-eighth of the energy provided by the power supply is stored in the magnetic field.

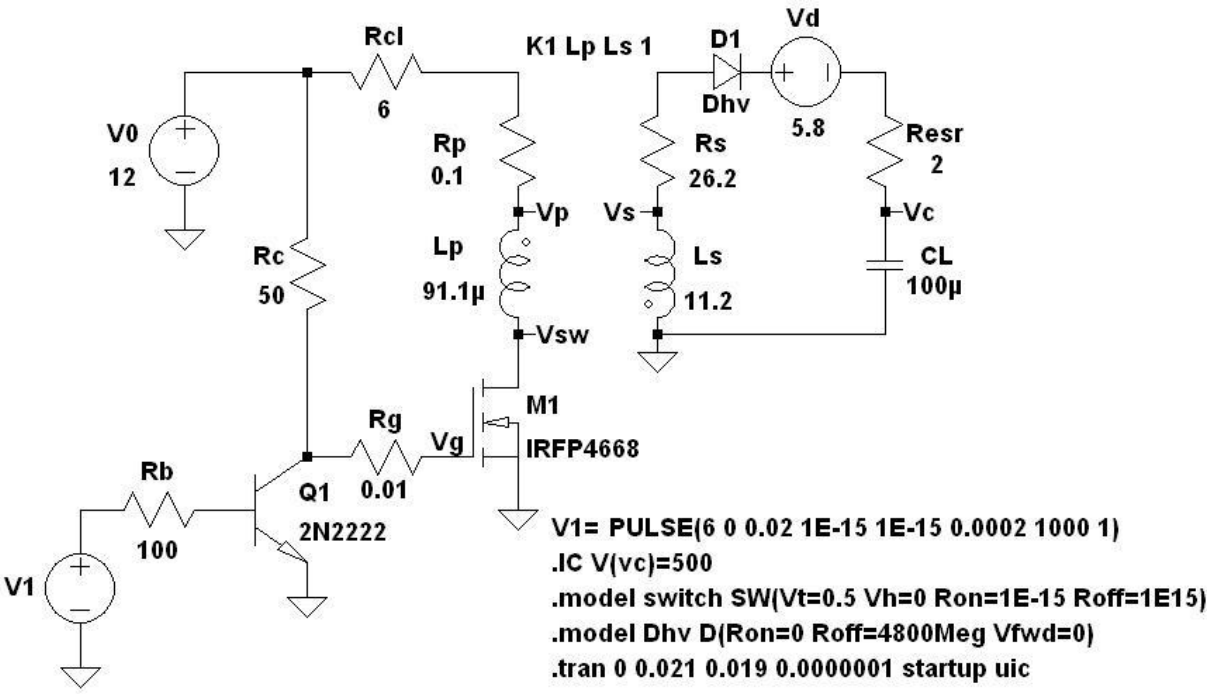
## Part #2B – A single discharging cycle; non-conducting phase

Notwithstanding that we have already completed Part #3, we should, as a formality, complete the analysis of the discharging cycle. We have already seen that the current flowing in the secondary circuit declines linearly with time during the conducting phase of the discharging cycle. Once the current reaches zero, at time $T_{stop}$, nothing further happens, in either the primary or secondary circuits. Remember that cutting off the primary circuit is what started the discharging cycle.

Since nothing happens during the non-conducting phase of the discharging cycle, it is simply a time of waiting. Obviously, we will want to minimize the time spent waiting.

## Part 4 – Adding a real MOSFET

In this part, we will use a real switch to control the primary circuit – an n-channel enhancement-mode MOSFET, the IFRP4886 from International Rectifier. It is shown as component $M_1$ in the following schematic diagram, along with its driver transistor $Q_1$. Although the MOSFET is shown explicitly, the sub-circuit which would control its timing is not. In the schematic, the base of transistor $Q_1$ is a pulsed voltage source $V_1$, which is connected to $Q_1$'s base through resistor $R_b$.




Our old friend, resistor $R_{on} = 0.03\Omega$, is now gone, having been incorporated as one of the properties of the IRFP4886. Charge is delivered to the IRFP4886's gate through resistor $R_g$, which is connected to the collector of its driver transistor $Q_1$, a common 2N2222 npn transistor. When transistor $Q_1$ is active, or in its saturation mode, its collector is pulled down to ground potential. That turns off the MOSFET.

For simulation purposes, $Q_1$'s base is driven directly by voltage source $V_1$. $V_1$ has a nominal voltage of $6\text{V}$. Note the SPICE directive for $V_1$. At the start of the simulation, $V_1$ is high, putting transistor $Q_1$ into saturation, and cutting off the MOSFET. As before, the first $20\text{ms}$ of the simulation is the time period during which the main power supply $V_0$ comes up to speed.

$20\text{ms}$ into the simulation, voltage source $V_1$ goes low. As will be explained, this allows $M_1$'s gate to drift high. Current will begin to flow through the primary circuit. The charging cycle gets under way.

$200\mu\text{s}$ later, at simulation time $20.2\text{ms}$, voltage source $V_1$ goes high once again. This cuts off the primary circuit and begins the discharging cycle. The results of the simulation are graphed for the $2\text{ms}$ period starting $19\text{ms}$ into the simulation. We will look at the waveforms after we explain what should happen.

The value of $Q_1$'s base resistor $R_b$ has been selected to set, or limit, the current flowing into $Q_1$'s base to approximately $100\text{mA}$. The datasheet for the 2N2222 shows that its base-emitter saturation voltage can be as high as $2\text{V}$ when the base is sinking $50\text{mA}$. If the base-emitter voltage is $2\text{V}$, then the voltage drop over $R_b$ will be $12\text{V} - 2\text{V} = 10\text{V}$ and the current flowing through $R_b$ will be equal to $10\text{V}/100\Omega = 100\text{mA}$.

When voltage source $V_1$ is high, with a voltage of $6\text{V}$, transistor $Q_1$ will be forward-biased. If $Q_1$ operates in its linear region, then the collector current should be equal to the base current multiplied by the transistor's dc-current gain $\text{h}_{\text{FE}}$. The datasheet for the 2N2222 shows that its dc-current gain is typically in the range 35-100. Even with the minimum value of dc-current gain (35), the voltage drop over the collector resistor $R_c$ would be equal to $35 \times 50\Omega \times 100\text{mA} = 175\text{V}$. This is not possible. The

impossibility will be resolved as follows: transistor $Q_1$ will not operate in its linear region, but in its saturation mode.

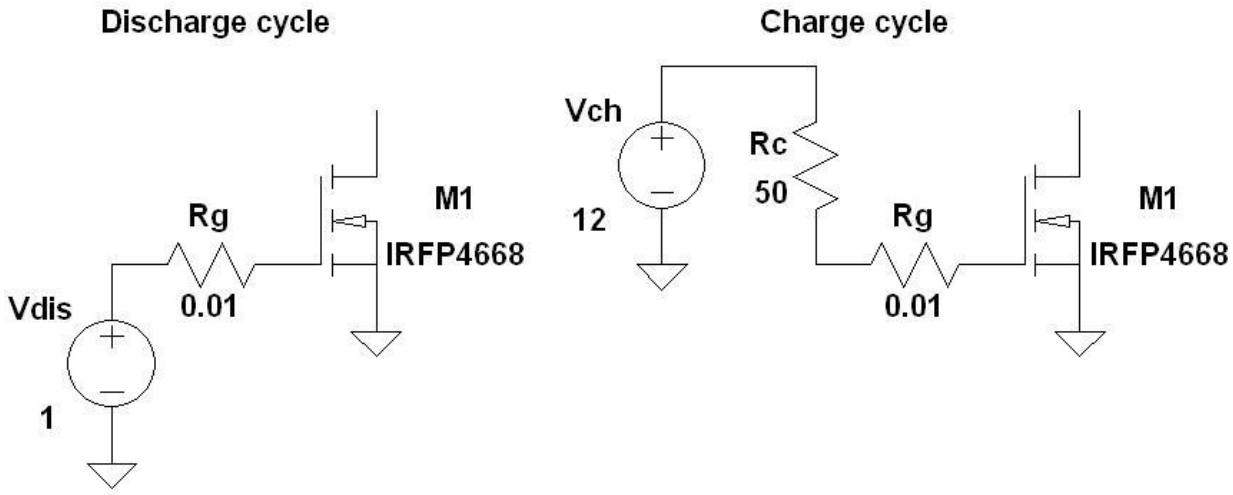
The datasheet for the 2N2222 shows that its collector-emitter voltage in saturation mode is a maximum of 1V when the base current is 50mA.

What all of this means is that, when the control voltage $V_1$ is high, the IRFP4886's gate is connected to a $1V$ voltage source though gate resistor $R_g = 0.01\Omega$. This should drain away the charge on the MOSFET's gate and turn it off.

Now, let us look at the case when the control voltage $V_1$ goes low. Transistor $Q_1$ will be cut off. In its cut-off mode, the collector terminal is free to float, and the voltage towards which the collector terminal will drift towards will be determined by the circuitry outside of the transistor. In our case, the collector terminal will be pulled up to the supply voltage ($V_0$) by the collector resistor $R_c$. The IRFP4886's gate will then be connected to a 12V voltage source through the series combination of $R_c$ and $R_g$. This should charge up the MOSFET's gate and turn it on.

The principal characteristic of the MOSFET's gate is its capacitance, and the charge it carries. Whereas a bipolar transistor is "on" when current flows into its base, a MOSFET is "on" when its gate capacitance is charged up. The speed with which the MOSFET is turned "on" and "off" is determined by the speed with which charge is added to, or removed from, its gate capacitance. The datasheet for the IRFP4886 shows that: (i) its total gate charge is typically 161nC, and (ii) its input capacitance is typically 10.72nF. Note that these two quantities are only consistent at a voltage of $V = Q/C = 15\text{V}$. I am told that it is better practice to use the gate charge in calculations and not to rely on the gate capacitance.

The following sub-schematics show the essential features of the IRFP4886 gate's charging and discharging circuits.



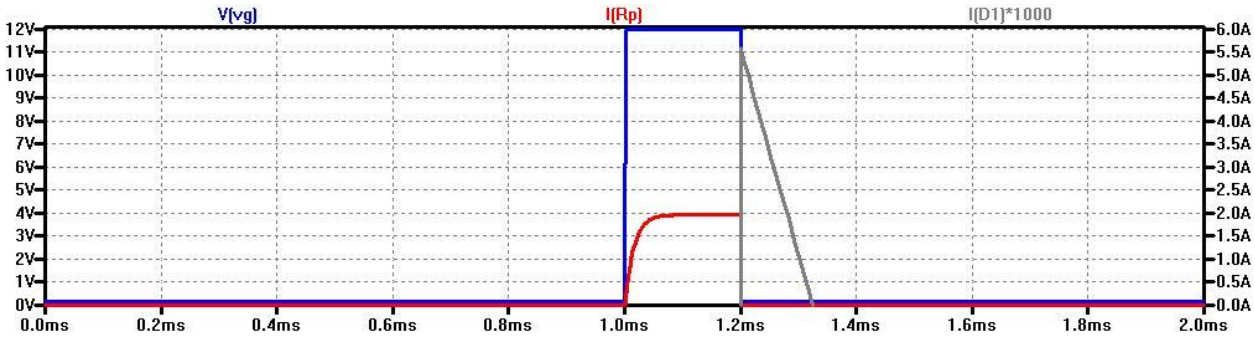

If the gate capacitance is 10.72nF, then the gate will discharge with a time-constant of $RC = 0.01 \times 10.72\text{n} = 0.11\text{ns}$. This is extremely fast. If the gate is initially charged up to 12V, then the initial discharge current will be $12\text{V}/0.01\Omega = 1200\text{A}$. This is extremely high, but the current will not last very long. In any event, the gate will discharge within five time-constants, being one-half nanosecond or so.

On the other hand, during charging, the gate will charge up with a time-constant of $RC = 50.01 \times 10.72\text{n} = 536\text{ns}$. If the gate is initially at zero volts, then the initial charging current will be equal to

$12\text{V}/50.01\,\Omega = 240\text{mA}$. In any event, the gate will charge up within five time-constants, being $2.5\mu\text{s}$ or so.

From an overall point-of-view, the MOSFET's gate is pulled down when transistor $Q_1$ is turned on and allowed to float up when transistor $Q_1$ is turned off. It would be possible to add another transistor, in a push-pull configuration with $Q_1$, so that the MOSFET's gate is both pushed and pulled. I do not believe this addition is necessary – the charge and discharge times seem to be suitably fast.

The following graph shows the result of the SPICE simulation. The variables shown are the MOSFET's gate voltage $v_g$ (the SPICE variable V(vg) is shown in blue), the primary current flowing through resistor $R_p$ (the SPICE variable I(Rp) is shown in red) and the secondary current flowing through diode $D_1$(the SPICE variable I(D1) is shown in gray). Note that the secondary current is multiplied by 1000 and is equal to about $5.5\text{mA}$ at the start of the discharging cycle.




All is as expected. The gate voltage rises from zero to $12\text{V}$ in a time frame too short to show on the graph. Once the MOSFET is turned on, the primary current rises to its steady-state value in less than $100\mu\text{s}$. When transistor $Q_1$ is turned on, the MOSFET's gate voltage decreases to zero instantaneously, at least on the scale visible in the chart. This begins the discharging cycle, during which the secondary current decreases almost linearly with time, consistent with our calculations above.

## Part 5 – Asynchronous operation with a 555 timer

In this section, we will look at the circuit with the timing controlled by a 555 timer wired for astable, or cyclic, operation. The timer will generate pulses of a fixed length and fixed duty cycle. This is going to require some compromise among things which do not have a fixed duration, and will therefore cause some loss of efficiency.

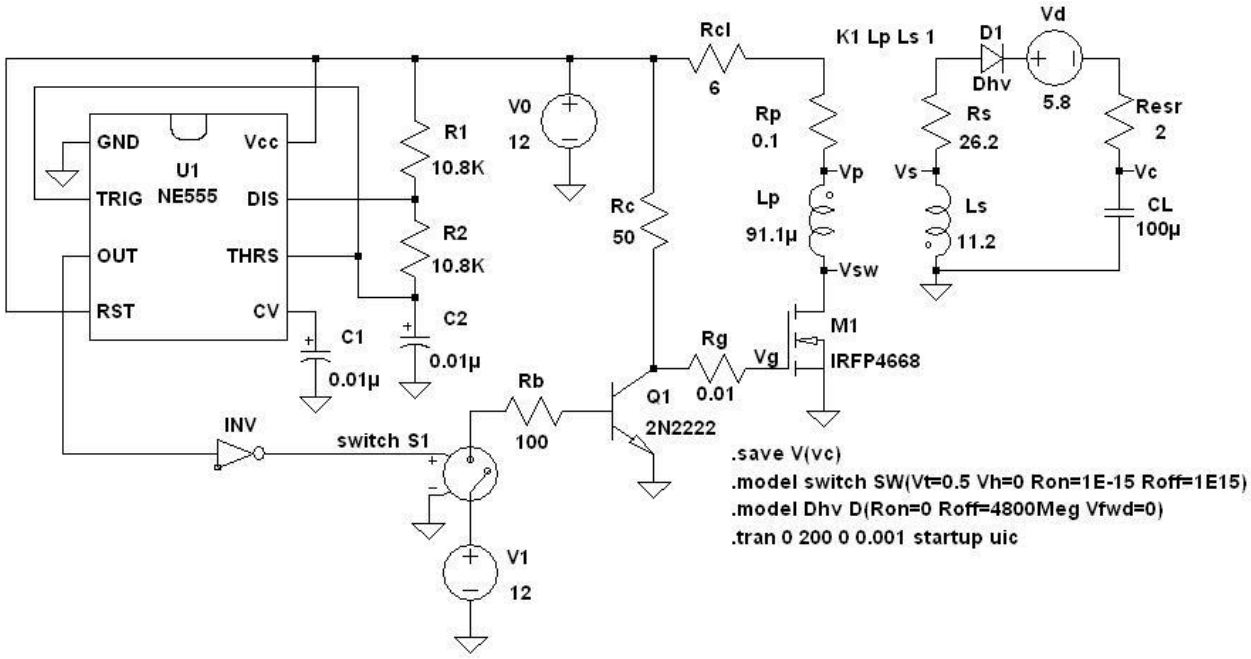
There will not be a problem with the charging cycle. We can easily configure the timer to generate pulses $74.5\mu\text{s}$ long, which will allow five $\tau_p$ time-constants for the charging cycle, during which the current flowing through the primary winding builds up to its steady-state value. The length of the charging cycle does not depend on the load capacitor's initial voltage, so the same length of pulse can be used during the entire charging procedure.

It is the discharging cycle which presents the problem. The length of the discharging cycle does depend on the capacitor's initial voltage. The length of the discharging cycle varies widely, from $10.22\text{ms}$ when the capacitor is uncharged, to $123.5\mu\text{s}$ at $500\text{V}$ and down to $20.79\mu\text{s}$ by the time the capacitor has reached $3000\text{V}$. No single length of time will suit all capacitor voltages.

If we end a discharging cycle before $T_{stop}$, by which time the secondary current has fallen to zero, then we waste energy. We will not have given the secondary circuit enough time to transfer all of the available energy from the magnetic field to the load capacitor.

On the other hand, if we wait until after $T_{stop}$ before beginning the next charging cycle, then we waste time in the non-conducting phase of the discharging cycle, when nothing happens at all.

Somewhat arbitrarily, I have selected a discharge period of $150\mu s$, twice the charging period of $75\mu s$. There is no magic to this selection. It happens that the capacitor voltage for which $150\mu s$ is the perfect $T_{stop}$ is $410.6V$. The following schematic diagram shows the circuit which we will simulate in this section.

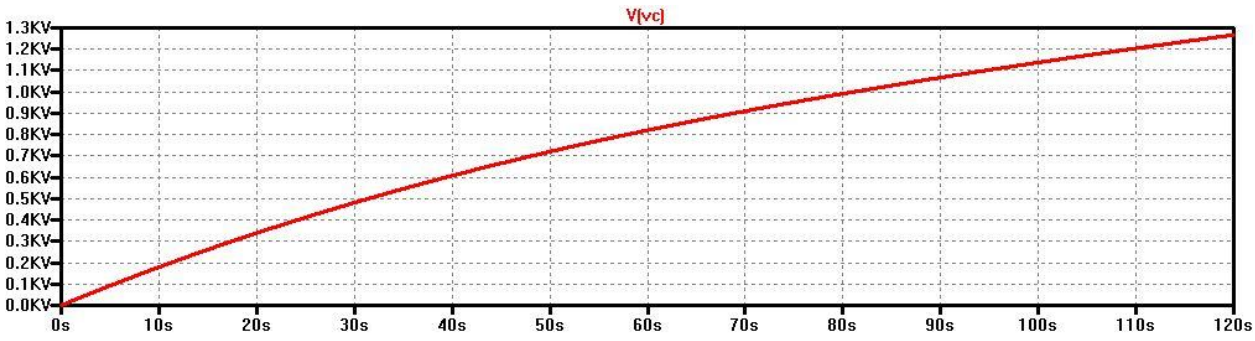



The 555 timer is wired as an astable. With the component values shown, its output pulse (see the datasheet) will have the following high and low times.

$$\begin{aligned} t_{high} &= 0.693 \times (10.8\text{K} + 10.8\text{K}) \times 0.01\mu = 149.7\mu s \\ t_{low} &= 0.693 \times 10.8\text{K} \times 0.01\mu = 74.8\mu s \end{aligned}$$

We need the MOSFET's gate to be high for the duration of the low pulse, which necessitates introducing an inverter into the timer's output line. The limitations of my version of SPICE require that the inverter's output, which is a logical 0-1 output, be scaled to 12V by using switch $S_1$ and voltage source $V_1$. A practical 12V inverter would not need such conversion.

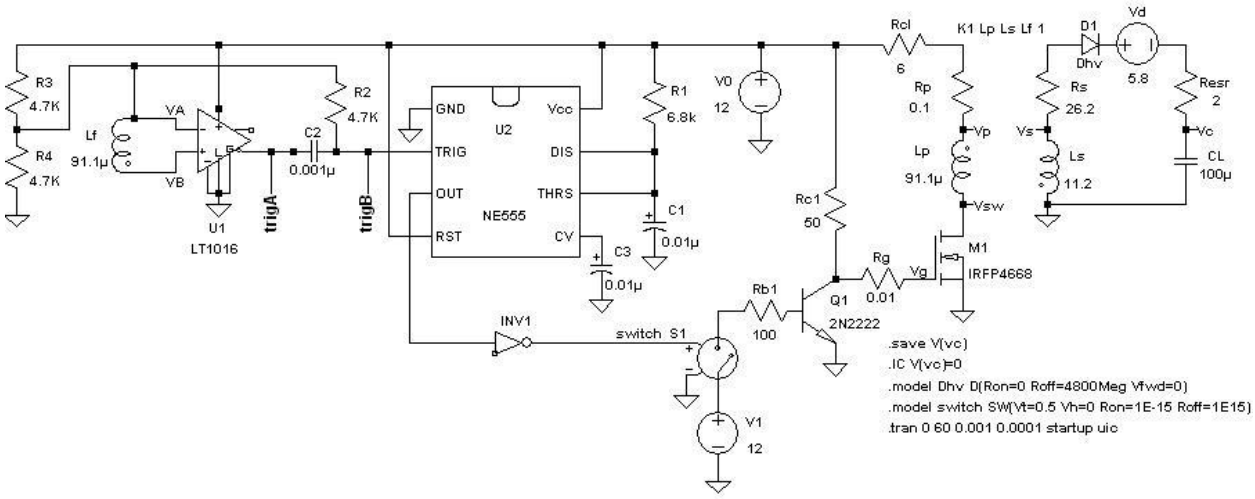
The following graph is the result of the SPICE simulation for the first $120s$ (yes – two minutes) of operation. The trace graphed is the voltage $v_c$ over the load capacitor (the SPICE variable V(vc) is shown in red).




At the end of two minutes, the voltage over the load capacitor is slightly more than 1250V.

## Part 6 – Controlling operation with a feedback winding

In this section, we will look at the following circuit, which includes a feedback mechanism. Near the left-hand side of the circuit, there is a coil labeled $L_f$. The subscript "$f$" stands for feedback. This coil is a third winding on the transformer.




The 555 timer is still in the circuit, but it controls the length of the charging cycle only. In this circuit, the 555 timer is wired as a monostable, "mono" meaning one pulse only. On a high-to-low transition of its trigger pin, the 555 timer generates a single high pulse at its output pin. The duration of the pulse is determined by resistor $R_1$ and capacitor $C_1$. With the component values shown, its output pulse (see the datasheet) will have the following duration:

$$t_{high} = 1.1 \times 6.8K \times 0.01\mu = 74.8\mu s$$

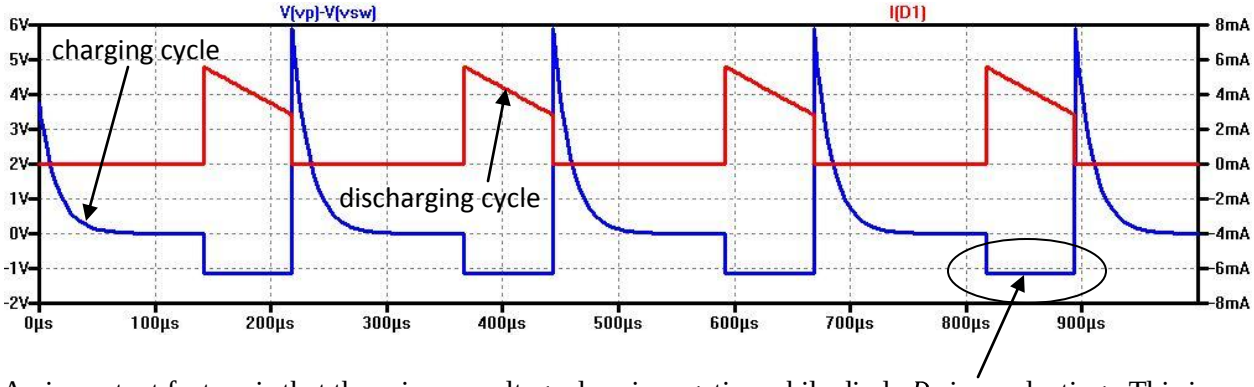
This is exactly the length of the five time-constants which we want the charging cycle to take.

Now, let us consider the transformer's third winding. It "feeds back" into the timing control circuit, certain information which identifies when the discharging cycle comes to an end. For convenience, I have set the self-inductance of the feedback winding to $L_f = 91.1\mu H$. This is the same as the self-inductance of the primary winding $L_p$. Physically, this means that the feedback winding will consist of three turns around the transformer's toroid core, just like the primary winding.

The ends of the feedback winding are connected to the two input terminals of a differential comparator, $U_1$, an LT1016. Since the input impedance of the comparator is very high, the feedback winding is close to being an open circuit and should place very little load on the primary circuit. The primary circuit should operate just as it has done in the previous sections of this paper.

What is important here is the voltage drop over the feedback winding. Since the feedback winding has a $1:1$ turns-ratio with the primary winding, the magnitude of the voltage drop over the feedback winding should be equal at all times to the voltage drop over the primary winding.

Let us step back for a moment and look at the event we are trying to detect. The following graph was produced for the circuit in the preceding section, in which the 555 timer controlled the circuit asynchronously. In this graph, the primary voltage drop $v_p - v_{sw}$ and secondary current $i_s$ are plotted for several complete charging and discharging cycles.

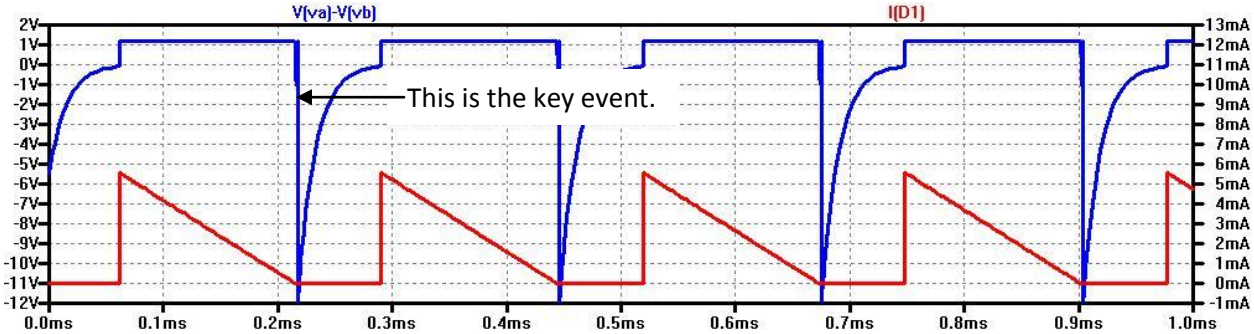



An important feature is that the primary voltage drop is negative while diode $D_1$ is conducting. This is the part of the trace inside the ellipse. At all other times, the primary voltage drop is positive. If we can detect when the primary voltage drop is negative, and in particular when it reverts from negative to positive, then we will know when the conducting phase of the discharging cycle ends. That is the moment when we should start a new charging cycle. (Note that I have scaled the secondary current, which is shown in red with its axis on the right-hand side, so that it does not interfere with the trace for the primary voltage drop, which is shown in blue with its axis on the left-hand side.)

Incidentally, this graph shows something else as well. Note that the current flowing through the secondary circuit is truncated before time $T_{stop}$ is reached. The secondary current is not allowed to decline all the way to zero. That is a limitation of the asynchronous control described in the previous section. Remember, setting fixed-length times for both the charging and the discharging cycle involved compromise. The waveform in the graph was produced with an initial capacitor voltage of $400\text{V}$, for which the selected discharging time is too short. Energy is wasted. That disadvantage is, of course, the motivation for developing the feedback mechanism in this section.

In the circuit of this section, the voltage drop over the primary winding is duplicated over the feedback winding. The following graph is based on the circuit in this section. It shows the voltage drop $v_A - v_B$ over the feedback winding and the secondary current for several complete cycles, once again starting with a capacitor voltage of $400\text{V}$. This time, the discharging cycle is permitted to continue until the secondary current reaches zero. (Once again, I have scaled the axis for the secondary current in this graph so that it does not interfere with the trace for the feedback voltage drop.)

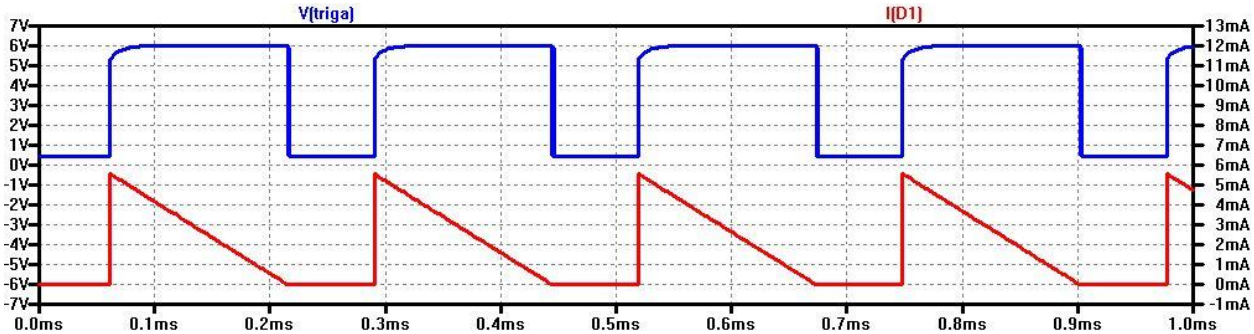
The voltage drop over the comparator $v_A - v_B$ has the same form as the voltage drop $v_p - v_{sw}$ over the primary winding. We will now describe how the comparator processes that voltage drop and causes a new charging cycle to begin.




The connection between the feedback winding and the comparator $U_1$ is such that the negative terminal of the comparator (voltage node $V_A$) is positive with respect to the positive terminal of the comparator (voltage node $V_B$) when the secondary circuit is conducting. This orientation must be correct or the circuit will not operate.

Resistors $R_3$ and $R_4$ constitute a simple 50% voltage divider. They cut the power supply's voltage in half and thereby provide a 6V reference voltage. In our circuit, the LT1016 comparator is wired up with a single voltage supply, as opposed to a dual voltage supply. In this configuration, the LT1016 will work best when the input voltages are near to the mid-point of its own power supply. Connecting the voltage divider's mid-point to one end of the feedback winding raises the "cross-over" voltage to 6V, so that it is well within the comparator's envelope of operation.

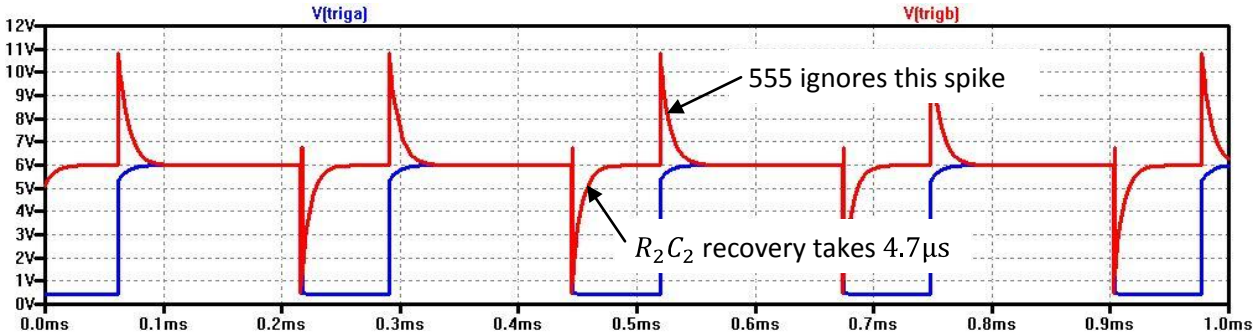
The purpose of the LT1016, once again, is to distinguish between positive and negative voltage drops over the feedback winding. The LT1016 has a binary output. When the voltage drop over the feedback winding is positive, the LT1016's output will be "high". When the feedback voltage drop is negative, the comparator's output will be "low". This shown in the following graph, which repeats the same conditions as the previous graph, but shows the output signal from the comparator (voltage node $\mathrm{Trig_A}$, shown in blue) along with the current flowing in the secondary circuit (shown in red).




The "high" output from the comparator is not 12V. Instead, it is the mid-point of the comparator's supply voltage, being only 6V. The "low" output is at ground potential. In some circuits, it would be necessary to compensate for this reduction in the voltage which corresponds to a logic "1". In our circuit, that is not necessary because the following component is a 555 timer, which is triggered by a high-to-low transition on its input pin. However, we do need to make sure that the high-to-low transition of the $\mathrm{Trig_A}$ waveform is interpreted by the 555 timer as a "one-off" high-to-low trigger pulse. It happens that a 555 timer which

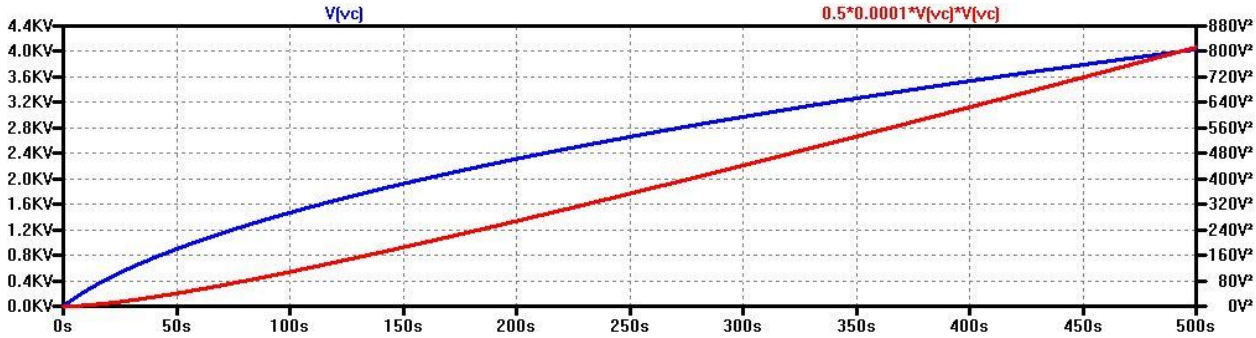
is powered by a 12V power supply will recognize and respond to a falling edge from 6V to ground just as well as it will recognize and respond to a falling edge from 12V to ground.

But, there is something else to be wary of. Successful operation of the 555 timer requires that the triggering pulse be shorter than the output pulse. Unexpected things can happen if the triggering waveform is still low when the output pulse comes to an end. Robust design requires that something be added to ensure that the trigger pulse returns to its high level, notwithstanding everything else. That is the purpose of resistor $R_2$ and capacitor $C_2$. Taken together, they have a time-constant equal to $\tau = R_2C_2 = (4.7\text{K})(0.001\mu) = 4.7\mu\text{s}$. The voltage at voltage node $\text{Trig}_\text{B}$ will rise from ground to 6V within about five time-constants, or $2.35\mu\text{s}$, regardless of what happens at voltage node $\text{Trig}_\text{A}$. This is shown in the following graph, which shows the voltages at voltage nodes $\text{Trig}_\text{A}$ and $\text{Trig}_\text{B}$ under the same conditions and for the same period of time as the two preceding graphs.




The operation of the $R_2$-$C_2$ pair is based on the principle that the voltage over capacitor $C_2$ cannot change instantaneously. This is handy because it gives rise to a sharp negative spike when the voltage at voltage node $\text{Trig}_\text{A}$ goes negative. On the other hand, it means there will be a similar sharp positive spike when the voltage at voltage node $\text{Trig}_\text{A}$ goes high once again. The 555 timer responds only to falling edges, and will ignore this positive spike.

The negative spike at voltage node $\text{Trig}_\text{B}$ triggers the 555 timer, which produces a pulse which remains high for $74.8\mu\text{s}$, as described above. While the output pulse from the 555 timer is high, transistor $Q_1$ is cut off, the voltage at the gate of MOSFET $M_1$ drifts high and the MOSFET conducts. Energy is stored in the magnetic field during this charging cycle. When the output pulse from the 555 timer ends, the primary circuit is cut off and the discharging cycle begins. At the end of the conducting phase of the discharging cycle, the secondary current reaches zero, the primary voltage drop reverts to a positive voltage, the feedback winding detects the change and the entire cycle begins once more. The following graph shows what happens.



This graph shows the operation of the circuit for 500 seconds, which is equal to eight minutes and 20 seconds, starting with an uncharged load capacitor. The blue trace is the voltage over the load capacitor, whose SPICE variable is V(vc). The red trace is the energy stored in the capacitor, with the SPICE symbols used in the equation $\frac{1}{2}C_L v_c^2$. It takes the circuit 500 seconds to charge the capacitor to the design voltage of 4000V and the design energy storage of 800J.

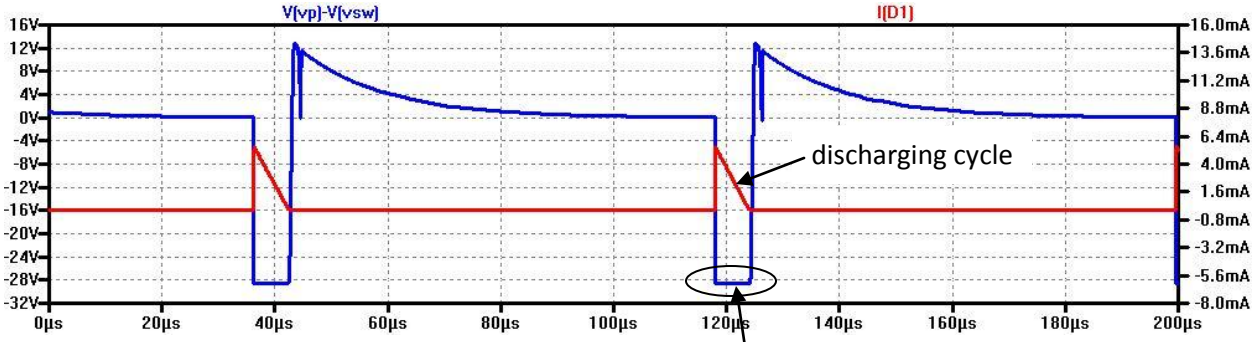
The charging process was going strong at 500 seconds, and the capacitor's voltage and energy would have continued to rise if I had let the simulation continue. (Incidentally, for most of this simulation, SPICE analyzed 1ms of simulation time during each second of real time. The run took about $500/0.001 = 500{,}000$ seconds, or five and three-quarters days. I did not want to wait any longer.)

## Part 7 – How does the "over-voltage" condition occur

It is clear that this circuit is able to charge the capacitor above the voltage determined by the classical transformer relationship. Once might expect that the voltage over the secondary winding could never exceed the voltage in the primary circuit (12V) multiplied by the square-root of the inductance ratio ($\sqrt{L_s/L_p} = \sqrt{11.2\text{H}/91.1\mu\text{H}}$). The product is equal to 4,208V. (Actually, I did let the simulation continue longer than 500 seconds, and the voltage over the load capacitor shoots through 4,208V quite nicely.)

I will call voltages greater than the classical transformer value "over-voltages". From the point-of-view of maximizing the energy stored in the load capacitor, over-voltages are fantastic. They are fantastic until one of the components exceeds its voltage rating and burns out.

In this section, I want to understand how this phenomenon occurs. The following graph shows the primary voltage drop and the secondary current for a 200µs period of time when the load capacitor is charged up to 10,000V. This voltage is far above the capabilities of the components I had envisioned using, but the circuit continues to operate.




During the conducting phase of the discharging cycle, the secondary current still starts off at about 5.8mA and declines linearly with time. (Once again, I have scaled the current axis so that the display of the current flowing through the diode does not obscure the voltage trace.) With the capacitor charged up to 10KV, Equation $(19')$ gives $T_{stop}$ as $6.25\mu s$. This is entirely consistent with what can be seen on the graph.

During this period, the voltage drop over the primary winding is about $-28.5$V. This is entirely consistent with the classical transformer requirement. The voltage over the secondary winding is 10KV, plus a few volts over diode $D_1$. The voltage ratio is equal $10{,}000/28.5 = 351$. This is the square-root of the inductance ratio: $\sqrt{11.2\text{H}/91.1\mu\text{H}} = 351$. All is as it should be.

The resolution to the conundrum is that the primary circuit is not "driving" the secondary circuit during this period of time. The voltage drop over the primary winding is not "causing" the voltage drop over the secondary winding in the manner of a traditional transformer. The voltage drop over the secondary winding is driven by something else.

That "something else" is the collapse of the magnetic field. The magnetic field is the source of the energy which gives rise to the voltage drops in both windings. When the magnetic field collapses at the end of the charging cycle, that energy must find somewhere else to go. It can flow out through either or both of the primary or secondary circuits. However, by turning off the MOSFET, we have effectively blocked off the primary circuit. Some leakage current can flow through the primary circuit, but only if it flows through the extremely high resistance of the inactive MOSFET. The easier route for the energy to escape through is the secondary circuit. If escape requires creating a high voltage over the secondary winding, so be it. It will create whatever voltage is needed over the secondary winding to allow the current to flow. The voltage that is needed for this purpose is equal to the sum of the load capacitor's voltage, the forward voltage drop over the diode and the Ohmic voltage drop developed as the current flows through the copper of the secondary winding.

As well as pumping current through the secondary winding, the collapsing field will pump some current through the primary winding as well. In fact, things will fall into place so that the ratio of the voltages over the secondary and primary windings is equal to the turns-ratio. In the case at hand, the 10KV over the secondary winding and the (negative) 28.5V over the primary winding are a perfect fit.

Achieving the necessary voltage drop over the primary winding is easy. Because of the extremely high resistance of the inactive MOSFET, extremely little current needs to flow through the MOSFET to offset the 28.5V or so that is dropped over the primary winding.

There is no theoretical limit to how high the voltage over the load capacitor can be raised. (Sorry, wrong wording. To be more precise, the components which we have included in the schematic do not present a theoretical limit. But, if we add some more theory, in the form of heating, electromagnetic radiation, changes in component values at high voltages and frequencies, then our mathematical model will better reflect reality and some limits will appear.)

## Part 8 – The time to reach full the design voltage

In this section, we will estimate the aggregate amount of time needed for the charging procedure to reach a particular voltage, beginning with an uncharged capacitor.

Let us consider the charging and discharging cycles which occur when the capacitor has reached a voltage of $v_c|_0$. The charging cycle takes a fixed period of time, $T_{charge}$, which we have set equal to five $\tau_p$ time-constants. The feedback mechanism ensures that the discharging cycle ends when its conducting period ends, at time $T_{stop}$, as expressed in Equation (19). During time $T_{charge} + T_{stop}$, the voltage over the capacitor increases by $\Delta v_c$ as expressed in Equation (29). For convenience, these quantities are repeated here.

$$\begin{aligned} T_{charge} &= 5\tau_p \\ T_{stop} &= \frac{\tau_s}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c|_0}{V_0}\right)\left(\frac{R_{\Sigma p}}{R_s + R_{esr}}\right) + 2}} \end{aligned} \quad (19)$$

and

$$\Delta v_c \quad = \frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c|_0}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2 \qquad (29)$$

The average change in the capacitor's voltage per unit of time during both cycles is therefore equal to:

$$\frac{\Delta v_c}{T_{charge} + T_{stop}} = \frac{\frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c|_0}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2}{5\tau_p + \frac{\tau_s}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c|_0}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 2}}$$

In the limit as the changes can be thought of as being very small, we can approximate this quantity as the derivative:

$$\frac{dv_c}{dt} \cong \frac{\frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2}{5\tau_p + \frac{\tau_s}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 2}}$$

The denominator can be re-organized to give:

$$\begin{aligned}
\frac{dv_c}{dt} \quad &\cong \frac{\frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2}{\frac{5\tau_p\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 10\tau_p + \tau_s}{\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 2}} \\
&= \frac{\frac{L_p}{2C_L}\left(\frac{1}{V_d + v_c}\right)\left(\frac{V_0}{R_{\sum p}}\right)^2\left[\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 2\right]}{5\tau_p\sqrt{\frac{L_s}{L_p}\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right)} + 10\tau_p + \tau_s} \\
&= \frac{\frac{L_p}{2C_L}\left(\frac{V_0}{R_{\sum p}}\right)^2\left[\frac{1}{V_0}\sqrt{\frac{L_s}{L_p}}\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right) + \left(\frac{2}{V_d + v_c}\right)\right]}{5\left(\frac{V_d + v_c}{V_0}\right)\left(\frac{\sqrt{L_p L_s}}{R_s + R_{esr}}\right) + 10\tau_p + \tau_s}
\end{aligned}$$

Then, re-arranging the two sides gives:

$$dt = \frac{5\left(\frac{v_c + V_d}{V_0}\right)\left(\frac{\sqrt{L_p L_s}}{R_s + R_{esr}}\right) + 10\tau_p + \tau_s}{\frac{L_p}{2C_L}\left(\frac{V_0}{R_{\sum p}}\right)^2\left[\frac{1}{V_0}\sqrt{\frac{L_s}{L_p}}\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right) + \left(\frac{2}{v_c + V_d}\right)\right]} dv_c$$

If we integrate this equation, starting with $v_c = 0$ at time $t = 0$, then we will have our required expression for the time needed to charge the capacitor up to voltage $v_c$.

$$T(v_c) = \int_{t=0}^{t=t} dt = \int_{v_c=0}^{v_c=v_c} \frac{5\left(\frac{v_c + V_d}{V_0}\right)\left(\frac{\sqrt{L_p L_s}}{R_s + R_{esr}}\right) + 10\tau_p + \tau_s}{\frac{L_p}{2C_L}\left(\frac{V_0}{R_{\sum p}}\right)^2\left[\frac{1}{V_0}\sqrt{\frac{L_s}{L_p}}\left(\frac{R_{\sum p}}{R_s + R_{esr}}\right) + \left(\frac{2}{v_c + V_d}\right)\right]} dv_c \quad (32)$$

Using our component values, the expression becomes:

$$\begin{aligned} T(v_c) &= \int_{v_c=0}^{v_c=v_c} \frac{5\left(\frac{v_c + 5.8}{12}\right)\left(\frac{\sqrt{(91.1\mu)(11.2)}}{26.2 + 2}\right) + 149\mu + 0.397}{\frac{91.1\mu}{200\mu}\left(\frac{12}{6.13}\right)^2\left[\frac{1}{12}\sqrt{\frac{11.2}{91.1\mu}}\left(\frac{6.13}{26.2 + 2}\right) + \left(\frac{2}{v_c + 5.8}\right)\right]} dv_c \\ &= \int_{v_c=0}^{v_c=v_c} \frac{\left(\frac{v_c + 5.8}{12}\right)(0.00566) + 149\mu + 0.397}{1.75\left[6.35 + \left(\frac{2}{v_c + 5.8}\right)\right]} dv_c \end{aligned}$$

I have not collapsed the terms. I want the interested reader to see that the $\tau_s$ term $(0.397)$ is the dominant constant in the numerator and that the term in the denominator which depends on $v_c$ is going to vanish at higher voltages. In any event, completing the arithmetic gives:

$$T(v_c) = \int_{v_c=0}^{v_c=v_c} \frac{0.000472 v_c + 0.400}{11.1 + \left(\frac{3.5}{v_c + 5.8}\right)} dv_c$$

If we ignore that term in the denominator which depends on $v_c$, then the integral can be written down by inspection as:

$$\begin{aligned} T(v_c \text{ Volts}) &= \frac{0.000472}{2 \times 11.1} v_c^2 + \frac{0.400}{11.1} v_c \\ &= 0.0000213 v_c^2 + 0.036 v_c \text{ seconds} \end{aligned}$$

When $v_c$ is expressed in KV, this becomes:

$$T(v_c \text{ KiloVolts}) = 21.3 v_c^2 + 36.0 v_c \text{ seconds}$$

To charge the capacitor up to 4KV should take $21.3(16) + 36.0(4) = 485$ seconds, which is almost exactly what we observed in the simulation. The graph of the simulation above shows the first $500$ seconds, and it is clear that the capacitor reaches 4KV a few simulation seconds before the end. Furthermore, the trace for $v_c$ in that graph seems slightly flatter than a square (meaning a square function, of form $y = x^2$, not a geometric square), which is due to the linear term $36.0v_c$.

Please see the accompanying documents for construction details and for a discussion about the effect of leakage in the transformer.

Jim Hawley
June 2012

An e-mail describing errors and omissions would be appreciated.